Instruction Based Management of Faulty Data Caches

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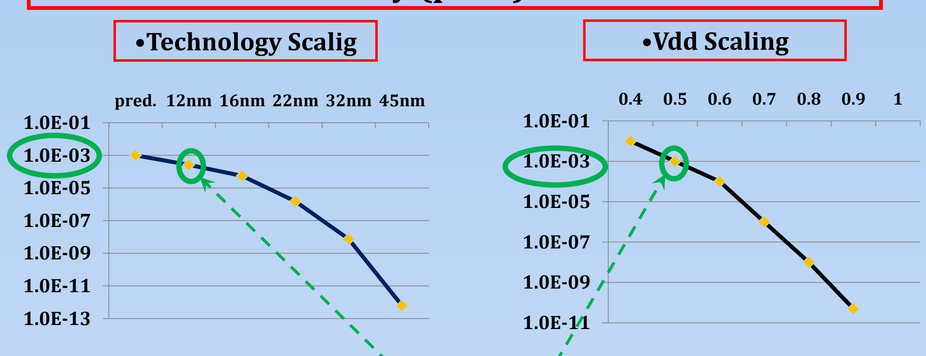
Motivation

1. Faulty Caches:

Technology and Vcc scaling → detriment impact in ICs reliability & yield management → performance degradation

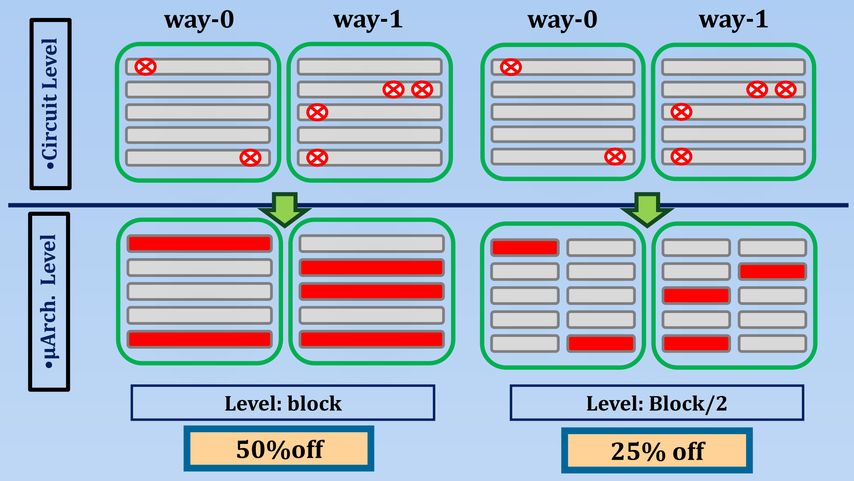
Failure Probability (pfail.) of SRAM Cells vs.



•Circuit level: pfail = $1{,}0*10^{-3}$ → 1 out of 1000 memory cells is faulty

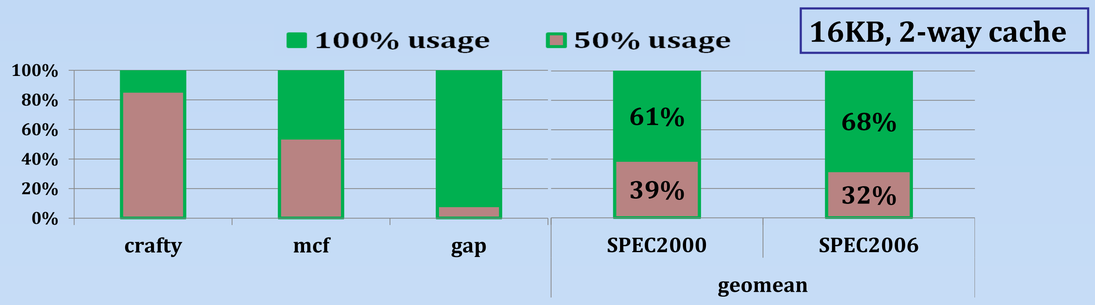
•Microarchitectural level → 43% reduction in effective cache capacity

2. Block Disabling (a.k.a., graceful degradation)

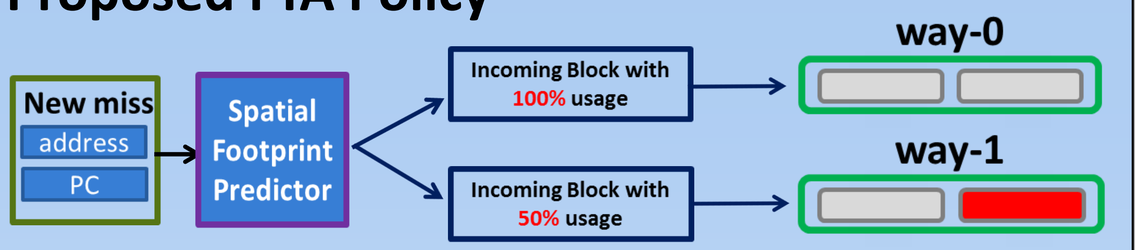


- Smaller block granularities → Larger fault-free memory capacity
- **Negligible Overheads**: One extra faulty bit indicator in every new granularity

3. Block Utilization Breakdowns

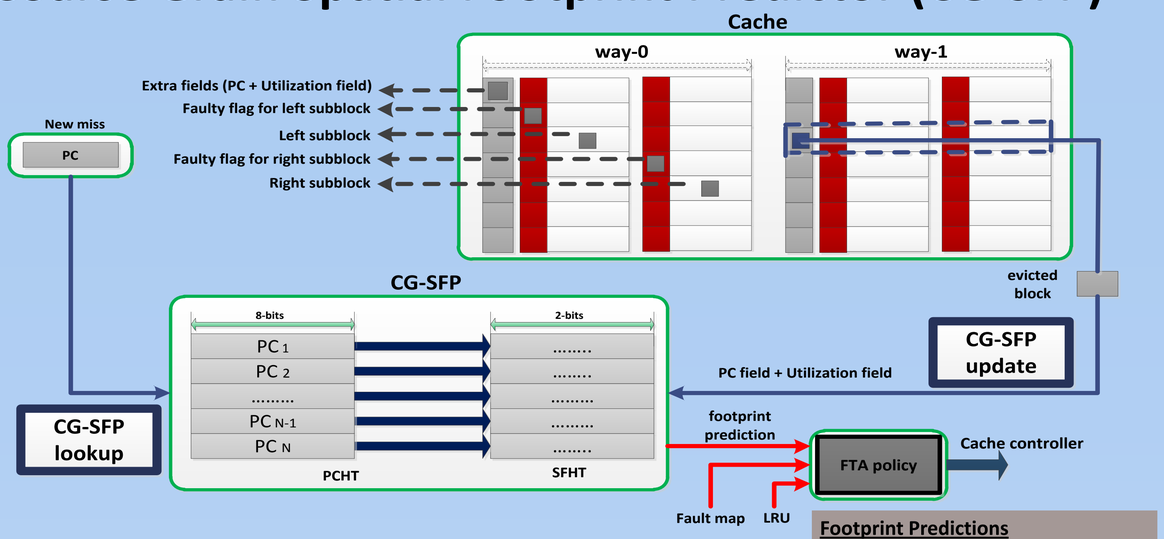


Proposed FTA Policy



- New Cache: fully functional, fully faulty & partially faulty frames
- Our approach: orchestrate cache accesses among various cache frames
- Hint: partially faulty cache frames ideal for block with limited spatial footprints → exploit **spatial locality**

Coarse Grain Spatial Footprint Predictor (CG-SFP)

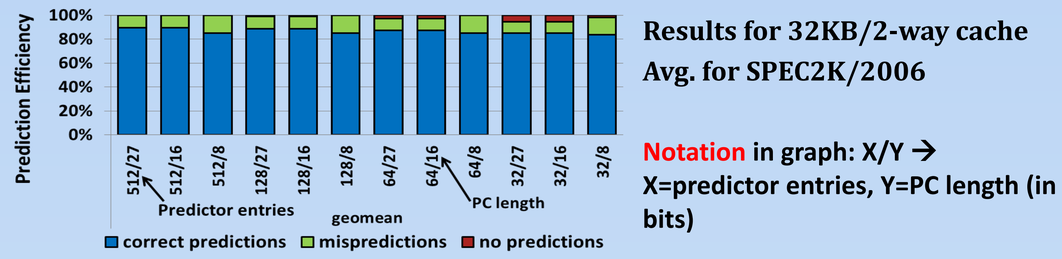


CG-SFP Basic Operations

- **Lookup→Input: PC of new miss, Output: spatial footprint prediction**
- **Update→Input: PC & footprint (utilization) field of just evicted blocks**

What about storage overhead?

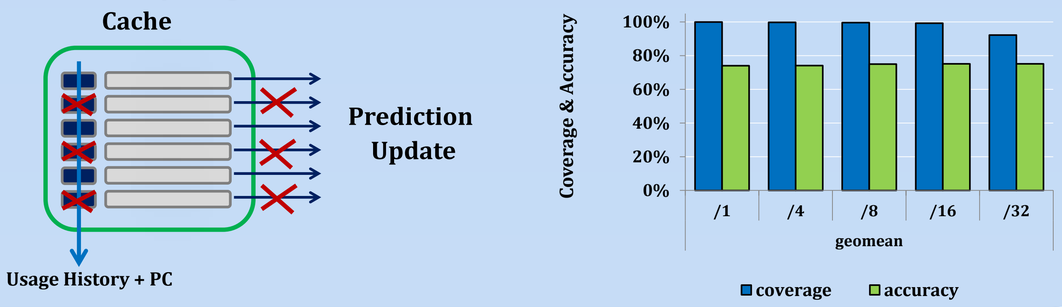
- **Reduce predictor entries and PC length**



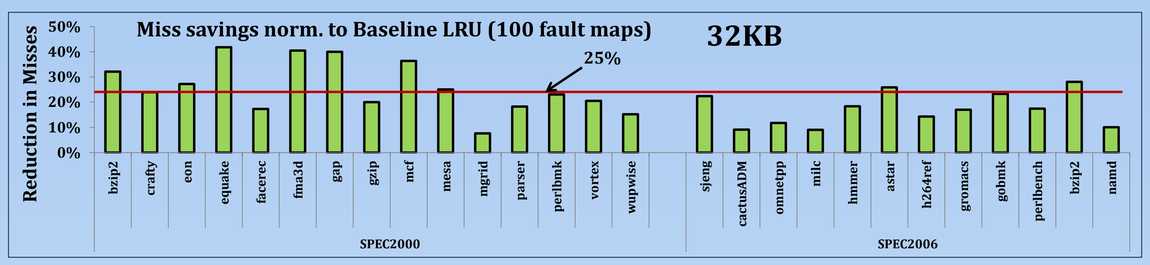
Results for 32KB/2-way cache
Avg. for SPEC2K/2006

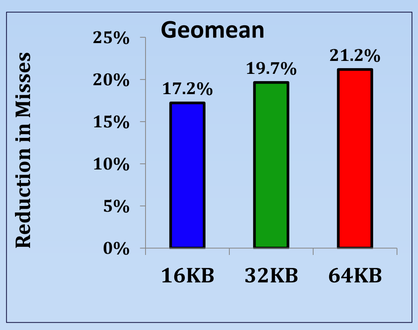
Notation in graph: X/Y → X=predictor entries, Y=PC length (in bits)

- **Set sampling:** Disregard some sets from predictor update operation



Results





- FTA policy clearly surpasses Baseline_LRU in all cases
- Top graph: from 42% (max) to 7.6% (min)
- Bottom left graph: well above 17% in all cache sizes

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Presented paper:

G. Keramidas, M. Mavropoulos et al. Spatial pattern prediction based management of faulty data caches. DATE, 2014.