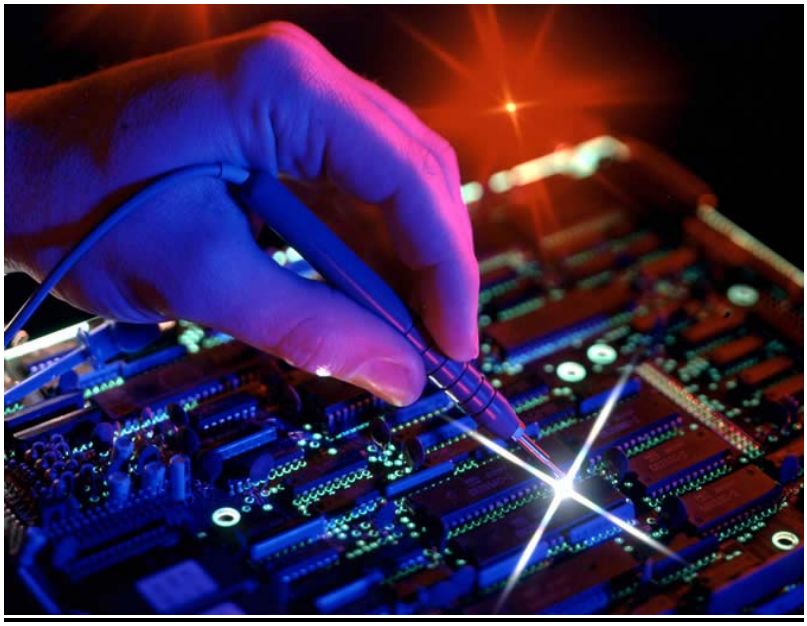
ΤΜΗΜΑ ΜΗΧΑΝΙΚΩΝ Η/Υ ΚΑΙ ΠΛΗΡΟΦΟΡΙΚΗΣ

ΠΑΝΕΠΙΣΤΗΜΙΟ ΠΑΤΡΩΝ

Οδηγός Μελέτης & Εκπόνησης Εργαστηρίου Ηλεκτρονικής ΙΙ

Δρ. Χ. Μιχαήλ –Δρ. Φ. Γκιουλέκας



Πάτρα, 2010

1. Γενικές Πληροφορίες

Το εργαστήριο Ηλεκτρονικής ΙΙ, είναι μάθημα του τετάρτου εξαμήνου και διεξάγεται στον εργαστηριακό χώρο απέναντι από την γραμματεία της σχολής, δηλαδή στον ίδιο χώρο που διεξάγονταν και το εργαστήριο της Ηλεκτρονικής Ι.

Το εργαστήριο διεξάγεται σε ομάδες των δύο ατόμων, και κάθε ομάδα θα εκπονήσει συνολικά πέντε εργαστηριακές ασκήσεις. Κάθε ομάδα θα προσέρχεται για εκπόνηση άσκησης, κάθε δεύτερη εβδομάδα σύμφωνα με το πρόγραμμα που έχει ανακοινωθεί. Για το ακαδημαϊκό έτος 2009-2010, τα εργαστήρια θα αρχίσουν από την Δευτέρα $1^{η}$ Μαρτίου.

Είναι προφανές ότι για να συμμετάσχει κάποιος με αξιώσεις στην διεξαγωγή του εργαστηρίου Ηλεκτρονικής ΙΙ, θα πρέπει να έχει συμμετάσχει με σχετική επιτυχία στην διεξαγωγή του εργαστηρίου Ηλεκτρονικής Ι, ώστε να γνωρίζει τον τρόπο σύνδεσης των στοιχείων, λειτουργία των γεννητριών και του παλμογράφου καθώς και την εν γένει λογική του εργαστηριακού εξοπλισμού. Σε κάθε περίπτωση όποιος δεν γνωρίζει τα παραπάνω, θα πρέπει να καταβάλει σημαντικό κόπο, πριν την αρχή του εργαστηρίου, ώστε να διαβάσει τα αντίστοιχα εγχειρίδια χρήσης και να κατατοπιστεί κατάλληλα. Ειδάλλως δεν θα είναι εφικτό για αυτόν να διενεργήσει της εργαστηριακές ασκήσεις.

2. Προεργασία Εργαστηριακών Ασκήσεων

Οι φοιτητές που θα προσέρχονται στο εργαστήριο για την διεξαγωγή της εργαστηριακής άσκησης είναι υποχρεωμένοι να έχουν μελετήσει την άσκηση πιο πριν. Θα πρέπει να έχουν μελετήσει τα κυκλώματα που θα υλοποιήσουν. Επειδή το εργαστήριο Ηλεκτρονικής ΙΙ, έχει να κάνει με την χρήση ολοκληρωμένων κυκλωμάτων οι φοιτητές πρέπει από το σπίτι τους να έχουν διαβάσει τα datasheets των αντίστοιχων ολοκληρωμένων που θα χρησιμοποιήσουν ώστε να ξέρουν τι λειτουργίες αυτό επιτελεί, ποιο ποδαράκι του ολοκληρωμένου αντιστοιχεί σε ποιον ακροδέκτη του κυκλώματος, τι πρέπει να συνδεθεί που και γιατί, κ.ο.κ. Σε αντίθετη περίπτωση δεν θα φτάσει ο χρόνος για να βρεθεί αυτή η πληροφορία κατά την διάρκεια εκπόνησης του εργαστηρίου και επίσης να φτιαχτούν τα κυκλώματα που προβλέπονται και να ληφθούν οι απαραίτητες μετρήσεις.

Επίσης θα πρέπει να έχετε προετοιμάσει το θεωρητικό κομμάτι της άσκησης, στο οποίο εν δυνάμει θα εξετάζεστε, σύμφωνα με αυτά που περιγράφονται στο εδάφιο 3. Κατόπιν παρατηρήσεων πολλών φοιτητών που συμμετείχαν στο εργαστήριο Ηλεκτρονικής Ι (ότι δεν έχουν διαβάσει τα αντίστοιχα θεωρητικά μαθήματα στα οποία βασίζεται το εργαστήριο, και για αυτό δεν μπορούσαν να κατανοήσουν την αντίστοιχη θεωρητική σημασία της), προσδιορίσαμε το εκπαιδευτικό υλικό και της πηγές του ώστε να έρχεστε προετοιμασμένοι κατάλληλα στα εργαστήρια (εδάφιο 3). Το υλικό αυτό προέρχεται είτε από το βιβλίο του μαθήματος των Ψηφιακών Ηλεκτρονικών που διδάσκεται στο Γ εξάμηνο ή από ελεγμένες πηγές του διαδικτύου. Αυτό το υλικό θα δίνεται και σαν παράρτημα στο τέλος αυτού του οδηγού για όσους από εσάς δεν έχετε συνεχή πρόσβαση στο διαδίκτυο.

Στο σύγγραμμα που θα προμηθευτείτε στο τέλος κάθε εργαστηριακής άσκησης υπάρχουν τα datasheets των περισσοτέρων από τα ολοκληρωμένα που θα χρησιμοποιήσετε στα πλαίσια των εργαστηριακών ασκήσεων. Υπάρχουν όμως και άλλα που αν και θα χρειαστείτε δεν υπάρχουν μέσα στο σύγγραμμα. Αυτά θα τα βρείτε πολύ εύκολα κάνοντας μια αναζήτησης στο διαδίκτυο (π. μέσω google), με όρους αναζήτησης τον τύπο του ολοκληρωμένου κυκλώματος , ακολουθούμενο από την λέξη datasheet. Π.χ. για το χρονιστή (timer) 555, που όπως αναφέρεται στην εργαστηριακή άσκηση 5, χρησιμοποιείται μέσω του ολοκληρωμένου LM555, αρκεί να γράψουμε σαν όρο αναζήτησης το "LM555 datasheet". Λογικά το datasheet που ψάχνεται θα βρίσκεται στη πρώτες επιλογές. Στα πλαίσια του εν λόγω οδηγού «Μελέτης και εκπόνησης Εργαστηρίου Ηλεκτρονικής ΙΙ», θα γίνει προσπάθεια ώστε στο τέλος του να υπάρχουν τα datasheets όλων των ολοκληρωμένων που θα χρειαστείτε.

Είναι πολύ **ΣΗΜΑΝΤΙΚΟ,** να έχετε μελετήσει τα datasheet των ολοκληρωμένων κάθε άσκησης πιο πριν, ώστε να ξέρετε σε τι αντιστοιχεί ο κάθε ακροδέκτης του ολοκληρωμένου και να μπορέσετε να φτιάξετε έστω τα κυκλώματα των εργαστηριακών ασκήσεων. Τα εν λόγω datasheet, δεν είναι ανάγκη να τα διαβάζετε στο σύνολο τους. Απλά να παίρνεται μόνο της απαραίτητες πληροφορίες για αυτά που αναφέρθηκαν πιο πάνω ώστε να μπορείτε να ανταποκριθείτε στης ανάγκες του εργαστηρίου σύμφωνα με τα ζητούμενα σε κάθε άσκηση.

3. Διδακτικό Υλικό Προεργασίας ανά Εργαστηριακή Άσκηση

Η εργαστηριακή άσκηση 1, περιέχει κυκλώματα που περιλαμβάνουν τελεστικούς ενισχυτές. Όλες της απαραίτητες πληροφορίες που θα χρειαστείτε τόσο για τα πρακτικά όσο για τα θεωρητικά ζητήματα του εργαστηρίου που αφορούν τους τελεστικούς ενισχυτές, θα της βρείτε στα ακόλουθα δύο links:

http://en.wikipedia.org/wiki/Operational_amplifier
http://en.wikipedia.org/wiki/Operational_amplifier_applications

Σε αυτά τα links, εξηγούνται εύκολα και κατανοητά όλα όσα απατούνται. Τελεστικούς ενισχυτές έχετε διδαχθεί και σε μαθήματα προηγούμενων εξαμήνων οπότε προφανώς σας καλύπτουν και τα αντίστοιχα συγγράμματα που χρησιμοποιήσατε σε αυτά τα μαθήματα. Θα χρειαστεί επίσης να μελετήσατε τα datasheets των ολοκληρωμένων LF411 και 741 που χρησιμοποιούνται στα πλαίσια της άσκησης.

Η εργαστηριακή άσκηση 2, περιέχει κυκλώματα που περιλαμβάνουν ψηφιακές πύλες, ταλαντωτές δακτυλίου (ring oscillators), πύλες TTL, πύλες CMOS και πύλες CMOS τριών καταστάσεων. Από άποψη υλικού που πρέπει να μελετήσετε είναι η πλέον εκτενής. Αυτό όμως θα το βρείτε μπροστά σας αφού και οι υπόλοιπες εργαστηριακές ασκήσεις στηρίζονται σε αυτές της γνώσεις. Έτσι εάν καταλάβετε της βασικές έννοιες αυτής της άσκησης θα έχετε ένα πολύ καλό εφόδιο για την συνέχεια του εργαστηρίου και λιγότερο διάβασμα στης επόμενες εργαστηριακές ασκήσεις.

Αυτά που θα χρειαστεί να μελετήσετε είναι τα αντίστοιχα εδάφια από το βιβλίο του μαθήματος των Ψηφιακών Ηλεκτρονικών του Γ εξαμήνου. Σε σχέση με το βιβλίο του κ. Λιούπη για τα Ψηφιακά Ηλεκτρονικά, θα πρέπει να μελετήσετε της σελίδες 23 έως 38 και 59 έως 63. το εν λόγω βιβλίο μπορεί να βρεθεί στην ηλεκτρονική διεύθυνση:

http://aiolos.cti.gr/gr/faculty/psifil/

και οι σελίδες που αναφέρονται πιο πάνω προς μελέτη ανήκουν στα κεφάλαια 2 και 3 αντίστοιχα. Πολλές και χρήσιμες πληροφορίες σχετικά με της λογικές πύλες, της πύλες τριών καταστάσεων κ.ο.κ, τους ταλαντωτές δακτυλίου κ.α. μπορείτε να βρείτε και στης ακόλουθες ιστοσελίδες:

http://en.wikipedia.org/wiki/Logic_gate
http://en.wikipedia.org/wiki/Ring_oscillator

Προφανώς μπορείτε να χρησιμοποιήσετε και συγγράμματα που έχετε πάρει από την σχολή και καλύπτουν τα παραπάνω θεματικά αντικείμενα. Θα χρειαστεί επίσης να μελετήσατε τα datasheets των ολοκληρωμένων 74LS00, 74HC00, και CD4007 που χρησιμοποιούνται στα πλαίσια της άσκησης.

Η εργαστηριακή άσκηση 3, περιέχει κυκλώματα που περιλαμβάνουν στοιχεία αποθήκευσης όπως latches, flip-flop τύπου D, T και J-K. Αυτά που θα χρειαστεί να διαβάσετε και να ξέρετε για την εκπόνηση του εργαστηρίου, βρίσκονται στης ακόλουθες ιστοσελίδες

http://en.wikipedia.org/wiki/Latch_(electronics)
http://en.wikipedia.org/wiki/Flip-flop_(electronics)

Προφανώς μπορείτε να χρησιμοποιήσετε και συγγράμματα που έχετε πάρει από την σχολή και καλύπτουν τα παραπάνω θεματικά αντικείμενα. Θα χρειαστεί επίσης να μελετήσατε τα datasheets των ολοκληρωμένων 74HC00, 74HC74, 74LS112, 74HC175, και 74HC08 που χρησιμοποιούνται στα πλαίσια της άσκησης.

Η εργαστηριακή άσκηση 4, διαπραγματεύεται την διασύνδεση λογικών πυλών ίδιων και διαφορετικών οικογενειών π.χ. διασύνδεση πυλών CMOS και TTL. Σε αυτή την άσκηση είναι απαραίτητο να γνωρίζετε αυτά που αναφέρθηκαν στην εργαστηριακή άσκηση 2 για της πύλες TTL και πύλες CMOS δηλαδή από το βιβλίο του μαθήματος των Ψηφιακών Ηλεκτρονικών του κ. Λιούπη της σελίδες 23 έως 38 και 59 έως 63. που ανήκουν στα κεφάλαια 2 και 3 αντίστοιχα.

Το μόνο νέο κομμάτι που θα πρέπει να μελετήσετε έχει να κάνει με το αντίστοιχο 4^{ο} κεφάλαιο του ίδιου βιβλίου που αφορά ακριβώς την διασύνδεση λογικών πυλών διαφορετικών οικογενειών. Έτσι πρέπει να διαβάσετε της σελίδες 91-95 από το αντίστοιχο τέταρτο κεφάλαιο.

Θα χρειαστεί επίσης να μελετήσατε τα datasheets των ολοκληρωμένων 74LS00, 74HC00, 74HCT00, 74LS04, 74HC04, CD4001B και CD400, που χρησιμοποιούνται στα πλαίσια της άσκησης.

Η εργαστηριακή άσκηση 5, περιέχει κυκλώματα που περιλαμβάνουν σκανδαλιστές Schmitt trigger και κυκλώματα χρονιστών. Για τον σκανδαλιστή Schmitt trigger, μπορείτε να διαβάσετε αρκετά πράγμα από της σελίδες 69-70 του βιβλίου του κ. Λιούπη για τα Ψηφιακά Ηλεκτρονικά καθώς επίσης και από την ακόλουθη ιστοσελίδα:

http://en.wikipedia.org/wiki/Schmitt_trigger

Όσον αφορά τον χρονιστή 555, υλικό προς μελέτη υπάρχει στης παρακάτω ιστοσελίδες:

http://en.wikipedia.org/wiki/555_timer_IC
http://www.doctronics.co.uk/555.htm

Προφανώς μπορείτε να χρησιμοποιήσετε και συγγράμματα που έχετε πάρει από την σχολή και καλύπτουν τα παραπάνω θεματικά αντικείμενα. Θα χρειαστεί επίσης να μελετήσατε τα datasheets των ολοκληρωμένων 74HC14, LM555, 7400, 74LS00, 74AS00, 74ALS00, 74HC00, 74AC00, 74LS04, CD4007, CD4001B και CD4050B, που χρησιμοποιούνται στα πλαίσια της άσκησης.

4. Εκπαιδευτικό Λογισμικό Εξομοίωσης Εργαστηριακών Ασκήσεων

Στα πλαίσια του εργαστηρίου θα δοθούν οδηγίες για την χρήσης εκπαιδευτικού λογισμικού για την εξομοίωση των εργαστηριακών ασκήσεων σε υπολογιστή κατ' οίκον. Αυτό θα μπορείτε να το χρησιμοποιείτε τόσο στο σπίτι για εξάσκηση, καθώς επίσης και για την περίπτωση όπου στα πλαίσια του εργαστηρίου κάποιοι από εσάς δεν προλάβουν να εκτελέσουν όλες της πειραματικές διατάξεις και να πάρουν όλες της μετρήσεις. Ο τρόπος αξιοποίησης αυτής της πρακτικής θα αναφερθεί στο εργαστήριο ώστε να εξασφαλιστεί ότι δεν θα υπάρχει περίπτωση όπου μια ομάδα θα πάρει απλά τα κυκλώματα και της μετρήσεις από κάποια άλλη ομάδα.

Το εκπαιδευτικό λογισμικό που συνίσταται αν χρησιμοποιήσετε είναι το "PSpice 9.1 Student Version", για το οποίο πιο κάτω θα αναφερθεί πιο συγκεκριμένο στοιχείο θα πρέπει να χρησιμοποιείται για κάθε ένα από τα ολοκληρωμένα κυκλώματα που χρησιμοποιούνται στα πλαίσια των εργαστηριακών ασκήσεων.

Το "PSpice 9.1 Student Version", μπορείτε να το κατεβάσετε από κάποια από τα δύο ακόλουθα links:

http://www.electronics-lab.com/downloads/schematic/013/
http://www.electronics-lab.com/downloads/cnt/fclick.php?fid=513

Για την χρήση του "PSpice 9.1 Student Version", θα βρείτε έναν τεράστιο όγκο πληροφοριών στο διαδίκτυο. Κατόπιν αναζήτησης στο διαδίκτυο, βρήκαμε ότι υπάρχει εξαιρετικό ελληνικό εκπαιδευτικό υλικό διαφόρων συναδέλφων που θα σας βοηθήσουν να μάθετε εύκολα και γρήγορα το εν λόγω εργαλείο. Αυτό το εκπαιδευτικό υλικό βρίσκεται στης ακόλουθες ιστοσελίδες:

http://www.ellab.physics.upatras.gr/content/view/162/2/lang,greek/
http://vergina.eng.auth.gr/kontoleon/Page-SPE.htm
http://vergina.eng.auth.gr/kontoleon/Page-SPD.htm

Παράλληλα στην προσωπική ιστοσελίδα του διδάσκοντα Χ. Μιχαήλ, υπάρχει οπτικοακουστικό υλικό (video-tutorials) για τον τρόπο χρήσης του συγκεκριμένου εργαλείου σε κυκλώματα vlsi. Ο τρόπος λειτουργίας του εργαλείου είναι ίδιος και απλά εσείς θα πρέπει να επιλέγετε τα κατάλληλα εξαρτήματα για τα κυκλώματα σας.

http://www.vlsi.ece.upatras.gr/~michail/vlsi/vlsi2.htm

Επίσης πολύ κατατοπιστικά, είναι και το ακόλουθα δύο εισαγωγικά κείμενα στην χρήση του "PSpice 9.1 Student Version".

www.ee.sharif.ir/~zandi/**PSpice**_Handbook.pdf
http://userweb.elec.gla.ac.uk/j/jdavies/orcad/spiceintro.pdf
http://denethor.wlu.ca/PSpice/pspice_tutorial.html#HI

Επιπλέον εκπαιδευτικό υλικό για την χρήση του "PSpice 9.1 Student Version", μπορείτε να βρείτε και στης ακόλουθες ιστοσελίδες, της οποίες ελέγξαμε και το υπάρχον υλικό είναι πολύ υψηλού επιπέδου:

http://www.ee.nmt.edu/~rison/ee321_fall02/Tutorial.html
http://cobweb.ecn.purdue.edu/~ee255/lecturesupp_files/PSpice-Tutorial.pdf
http://www.engr.colostate.edu/ECE562/Pspicetutorial.pdf
http://www.uta.edu/ee/hw/pspice/
http://ewh.ieee.org/soc/es/Nov1999/02/BEGIN.HTM

Πιο κάτω θα βρείτε της αντιστοιχίες μεταξύ των στοιχείων κάθε εργαστηριακής άσκησης και του αντίστοιχου στοιχείου που θα πρέπει να χρησιμοποιηθεί από τα διαθέσιμα στο "PSpice 9.1 Student Version", ώστε να μπορείτε εύκολα και γρήγορα να υλοποιείστε τα απαιτούμενα κυκλώματα.

ΑΣΚΗΣΗ 1

ΟΛΟΚΛΗΡΩΜΕΝΟ ΕΡΓΑΣΤΗΡΙΟΥ	ΜΟΝΤΕΛΟ ΤΟΥ SPICE
OPAMP LF411	**LF411**
OPAMP LM 741CN	**uA741**
Ροοστάτης	**R_var**

ΑΣΚΗΣΗ 2

ΟΛΟΚΛΗΡΩΜΕΝΟ ΕΡΓΑΣΤΗΡΙΟΥ	ΜΟΝΤΕΛΟ ΤΟΥ SPICE
SN74LS00	**7400**
SN74HC00	**7400**
D1N4148	**D1N4148**
CD4007	**Χρησιμοποιήσατε τα MOSFET τρανζίστορς MbreakN3D και MbreakP3D για να οργανώσετε τη συνδεσμολογία που απαιτείται**

ΑΣΚΗΣΗ 3

ΟΛΟΚΛΗΡΩΜΕΝΟ ΕΡΓΑΣΤΗΡΙΟΥ	ΜΟΝΤΕΛΟ ΤΟΥ SPICE
SN74HC00	**7400**
SN74HC74	**7474**
SN74LS112	**74111**
SN74HC08	**7408**
SN74HC175	**74175**

ΑΣΚΗΣΗ 4

ΟΛΟΚΛΗΡΩΜΕΝΟ ΕΡΓΑΣΤΗΡΙΟΥ	ΜΟΝΤΕΛΟ ΤΟΥ SPICE
SN74LS00	**7400**
SN74HC00	**7400**
D1N4148	**D1N4148**
SN74HC08	**7408**
SN74LS04	**7404**
SN74HC04	**7404**
CD4050B	**7433 ή 7402**

ΑΣΚΗΣΗ 5

ΟΛΟΚΛΗΡΩΜΕΝΟ ΕΡΓΑΣΤΗΡΙΟΥ	ΜΟΝΤΕΛΟ ΤΟΥ SPICE
SN74HC00	**7400**
SN74HC14	**7414**
Zener Diode	**DIN750 Ή 1N4370A**
LM555	**555D**
SN74LS00	**7400**
SN74HC00	**7400**
CD4050B	**7433 ή 7402**
CD4001B	**7433 ή 7402**
CD4007	**Χρησιμοποιήσατε τα MOSFET τρανζίστορς MbreakN3D και MbreakP3D για να οργανώσετε τη συνδεσμολογία που απαιτείται**

Σημ:
Στην περίπτωση που εισάγετε Flip-Flop στο schematics για να πραγματοποιηθεί η εξομοίωση θέσατε την αρχική τους κατάσταση ως ακολούθως:

Analysis->Digital Setup και επιλέγετε> Flip-Flop Initialization All 1 Default A/D interface ->Level

Κατόπιν όλων αυτών που έχουν αναφερθεί πιο πάνω θεωρούμε ότι πλέον έχετε όλα τα απαραίτητα εφόδια, ανεξαρτήτως των μαθημάτων προηγούμενων εξαμήνων που έχετε ή δεν έχετε διαβάσει, ώστε να εκτελέσετε σωστά της εργαστηριακές ασκήσεις κατανοώντας και το αντίστοιχο θεωρητικό υπόβαθρο.

Σας ευχόμαστε καλή επιτυχία…

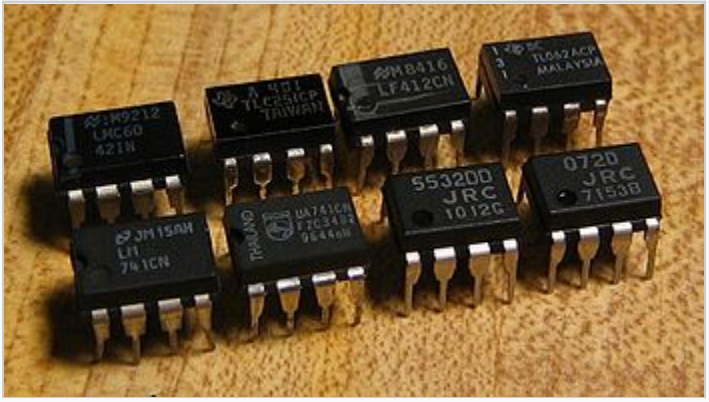
Οι Διδάσκοντες

Δρ. Χαράλαμπος Μιχαήλ
Δρ. Φώτιος Γκιουλέκας

ΠΑΡΑΡΤΗΜΑΤΑ ΜΕΛΕΤΗΣ ΕΡΓΑΣΤΗΡΙΟΥ ΗΛΕΚΤΡΟΝΙΚΗΣ ΙΙ

Operational amplifier

From Wikipedia, the free encyclopedia



Various op-amp ICs in eight-pin dual in-line packages ("DIPs")

An **operational amplifier**, which is often called an **op-amp**, is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output.[1] An op-amp produces an output voltage that is typically millions of times larger than the voltage *difference* between its input terminals.

Typically the op-amp's very large gain is controlled by negative feedback, which largely determines the magnitude of its output ("closed-loop") voltage gain in amplifier applications, or the transfer function required (in analog computers). Without negative feedback, and perhaps with positive feedback for regeneration, an op-amp essentially acts as a comparator. High input impedance at the input terminals (ideally infinite) and low output impedance at the output terminal(s) (ideally zero) are important typical characteristics.

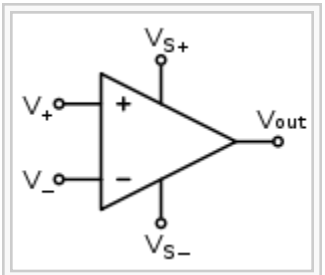
Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices. Many standard IC op-amps cost only a few cents in moderate production volume; however some integrated or hybrid operational amplifiers with special performance specifications may cost over $100 US in small quantities. Op-amps sometimes come in the form of macroscopic components, (see photo) or as integrated circuit cells; patterns that can be reprinted several times on one chip as part of a more complex device.

The op-amp is one type of differential amplifier. Other types of differential amplifier include the fully differential amplifier (similar to the op-amp, but with two outputs), the instrumentation amplifier (usually built from three op-amps), the isolation amplifier (similar to the instrumentation amplifier, but which works fine with common-mode voltages that would destroy an ordinary op-amp), and negative feedback amplifier (usually built from one or more op-amps and a resistive feedback network).

Contents

Circuit notation

The circuit symbol for an op-amp is shown to the right, where:



Circuit diagram symbol for an op-amp

- V_+: non-inverting input
- V_-: inverting input
- V_{out}: output
- V_{S+}: positive power supply
- V_{S-}: negative power supply

The power supply pins (V_{S+} and V_{S-}) can be labeled in different ways (*See IC power supply pins*). Despite different labeling, the function remains the same — to provide additional power for amplification of signal. Often these pins are left out of the diagram for clarity, and the power configuration is described or assumed from the circuit.

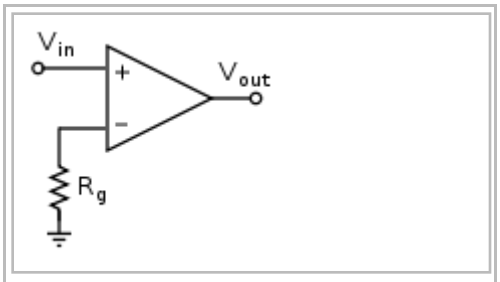
Operation

The amplifier's differential inputs consist of a V_+ input and a V_- input, and ideally the op-amp amplifies only the difference in voltage between the two, which is called the *differential input voltage*. The output voltage of the op-amp is given by the equation,

$$V_{\text{out}} = (V_+ - V_-)\, G_{\text{open-loop}}$$

where V_+ is the voltage at the non-inverting terminal, V_- is the voltage at the inverting terminal and $G_{\text{open-loop}}$ is the open-loop gain of the amplifier. (The term open-loop refers to the absence of a feedback loop from the output to the input.)

The magnitude of $G_{\text{open-loop}}$ is typically very large—seldom less than a million—and therefore even a quite small difference between V_+ and V_- (a few microvolts or less) will result in amplifier saturation, where the output voltage goes to either the extreme maximum or minimum end of its range, which is set approximately by the power supply voltages. *Finley's law* states that "When the inverting and non-inverting inputs of an op-amp are not equal, its output is in saturation." Additionally, the precise magnitude of $G_{\text{open-loop}}$ is not well controlled by the manufacturing process, and so it is impractical to use an operational amplifier as a stand-alone differential amplifier. If linear operation is desired, negative feedback must be used, usually achieved by applying a portion of the output voltage to the inverting input. The feedback enables the output of the amplifier to keep the inputs at or near the same voltage so that saturation does not occur. Another benefit is that if much negative feedback is used, the circuit's overall gain and other parameters become determined more by the feedback network than by the op-amp itself. If the feedback network is made of components with relatively constant, predictable, values such as resistors, capacitors and inductors, the unpredictability and inconstancy of the op-amp's parameters (typical of semiconductor devices) do not seriously affect the circuit's performance.

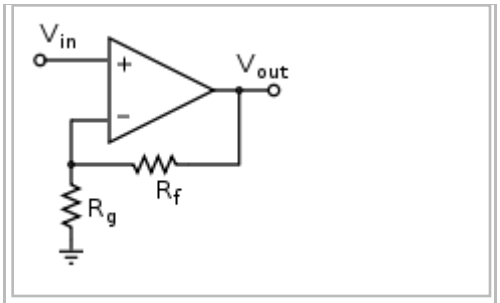


With no negative feedback, the op-amp acts as a switch. The inverting input is held at ground (0 V) by the resistor, so if the V_{in} applied to the non-inverting input is positive, the output will be maximum positive, and if V_{in} is negative, the output will be maximum negative. Since there is no feedback from the output to either input, this is an *open loop* circuit. The circuit's gain is just the $G_{\text{open-loop}}$ of the op-amp.

If no negative feedback is used, the op-amp functions as a switch or comparator.

Positive feedback may be used to introduce hysteresis or oscillation.

Returning to a consideration of linear (negative feedback) operation, the high open-loop gain and low input leakage current of the op-amp imply two "golden rules" that are highly useful in analysing linear op-amp circuits.



Adding negative feedback via R_f reduces the gain. Equilibrium will be established when V_{out} is just sufficient to reach around and pull the inverting input to the same voltage as V_{in}. As a simple example, if V_{in} = 1 V and R_f = R_g, V_{out} will be 2 V, the amount required to keep V_- at 1 V. Because of the feedback provided by R_f, this is a *closed loop* circuit. Its over-all gain V_{out} / V_{in} is called the *closed-loop gain* $G_{closed\text{-}loop}$. Because the feedback is negative, in this case $G_{closed\text{-}loop}$ is less than the $G_{open\text{-}loop}$ of the op-amp.

Golden rules of op-amp negative feedback

If there is negative feedback and **if** the output is not saturated,

1. both inputs are at the same voltage;
2. no current flows in or out of either input.[2]

These rules are true of the ideal op-amp and for practical purposes are true of real op-amps unless very high-speed or high-precision performance is being contemplated (in which case account must be taken of things such as input capacitance, input bias currents and voltages, finite speed, and other op-amp imperfections, discussed in a later section.)

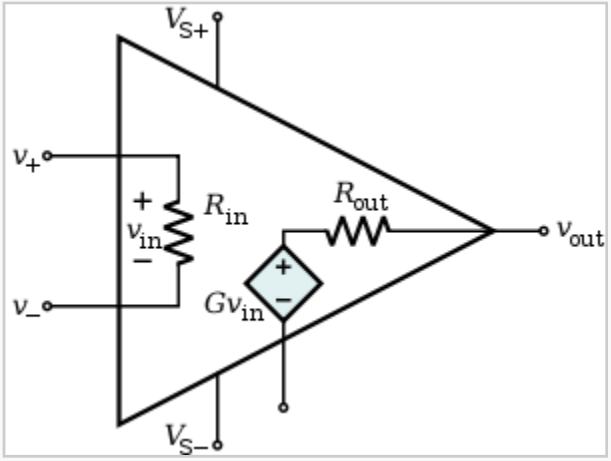
As a consequence of the first rule, the input impedance of the two inputs will be nearly infinite. That is, even if the open-loop impedance between the two inputs is low, the closed-loop input impedance will be high because the inputs will be held at nearly the same voltage. This impedance is considered as infinite for an ideal opamp and is about one megohm in practice.

Real and Ideal op-amps

Shown on the right is an equivalent circuit model of an operational amplifier. The main part in the amplifier is the dependent voltage source that increases in relation to the voltage across R_{in}, thus amplifying the voltage difference between V_+ and V_-.

Supply voltages V_{S+} and V_{S-} are used internally to power the dependent voltage source. The positive supply V_{S+} sets an upper bound on the output, and the negative source V_{S-} sets a lower bound on the output.

More sophisticated equivalent circuit models can also be constructed which include things such as input capacitance and input bias. On the other hand, one can imagine an even simpler "ideal" op-amp by assuming R_{in} to be infinite and $R_{\text{out}} = 0$.



Equivalent circuit of an operational amplifier.

An ideal op-amp is usually considered to have the following properties, and they are considered to hold for any input voltages:

- Infinite open-loop gain (i.e., when doing theoretical analysis, limit should be taken as open loop gain $G_{\text{open-loop}}$ goes to infinity)
- Infinite bandwidth (i.e., the frequency magnitude response is flat everywhere with zero phase shift).
- Infinite input impedance (so, in the diagram, $R_{\text{in}} = \infty$, and zero current flows from V_+ to V_-)
- Zero input current (i.e., there is no leakage or bias current into the device)
- Zero input offset voltage (i.e., when the input terminals are shorted so that $V_+ = V_-$, the output is a virtual ground).
- Infinite slew rate (i.e., the rate of change of the output voltage is unbounded) and power bandwidth (full output voltage and current available at all frequencies).
- Zero output impedance (i.e., $R_{\text{out}} = 0$, and so output voltage does not vary with output current)
- Zero noise
- Infinite Common-mode rejection ratio (CMRR)
- Infinite Power supply rejection ratio for both power supply rails.

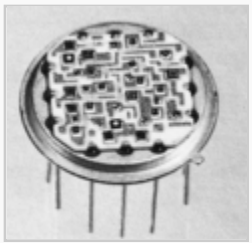
Because of these properties, an op-amp can be modeled as a nullor.

History

GAP/R's K2-W: a vacuum-tube op-amp (1953).

1941: First (vacuum tube) op-amp

An op-amp, defined as a general-purpose, DC-coupled, high gain, inverting feedback amplifier, is first found in US Patent 2,401,779 "Summing Amplifier" filed by Karl D. Swartzel Jr. of Bell labs in 1941. This design used three vacuum tubes to achieve a gain of 90dB and operated on voltage rails of ±350V. It had a single inverting input rather than differential inverting and non-inverting inputs, as are common in today's op-amps. Throughout World War II, Swartzel's design proved its value by being liberally used in the M9 artillery director designed at Bell Labs. This artillery director worked with the SCR584 radar system to achieve extraordinary hit rates (near 90%) that would not have been possible otherwise.[3]


ADI's HOS-050: a high speed hybrid IC op-amp (1979).

An op-amp in a modern DIP.

1947: First op-amp with an explicit non-inverting input

In 1947, the operational amplifier was first formally defined and named in a paper by Professor John R. Ragazzini of Columbia University. In this same paper a footnote mentioned an op-amp design by a student that would turn out to be quite significant. This op-amp, designed by Loebe Julie, was superior in a variety of ways. It had two major innovations. Its input stage used a long-tailed triode pair with loads matched to reduce drift in the output and, far more importantly, it was the first op-amp design to have two inputs (one inverting, the other non-inverting). The differential input made a whole range of new functionality possible, but it would not be used for a long time due

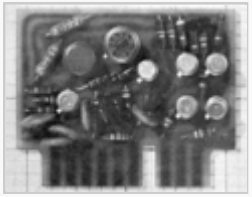
to the rise of the chopper-stabilized amplifier.[4]

1949: First chopper-stabilized op-amp

In 1949, Edwin A. Goldberg designed a chopper-stabilized op-amp.[5] This set-up uses a normal op-amp with an additional AC amplifier that goes alongside the op-amp. The chopper gets an AC signal from DC by switching between the DC voltage and ground at a fast rate (60 Hz or 400 Hz). This signal is then amplified, rectified, filtered and fed into the op-amp's non-inverting input. This vastly improved the gain of the op-amp while significantly reducing the output drift and DC offset. Unfortunately, any design that used a chopper couldn't use their non-inverting input for any other purpose. Nevertheless, the much improved characteristics of the chopper-stabilized op-amp made it the dominant way to use op-amps. Techniques that used the non-inverting input regularly would not be very popular until the 1960s when op-amp ICs started to show up in the field.

In 1953, vacuum tube op-amps became commercially available with the release of the model K2-W from George A. Philbrick Researches, Incorporated. The designation on the devices shown, GAP/R, is a contraction for the complete company name. Two nine-pin 12AX7 vacuum tubes were mounted in an octal package and had a model K2-P chopper add-on available that would effectively "use up" the non-inverting input. This op-amp was based on a descendant of Loebe Julie's 1947 design and, along with its successors, would start the widespread use of op-amps in industry.

1961: First discrete IC op-amps

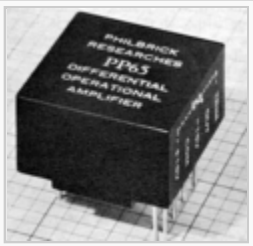


GAP/R's model P45: a solid-state, discrete op-amp (1961).

With the birth of the transistor in 1947, and the silicon transistor in 1954, the concept of ICs became a reality. The introduction of the planar process in 1959 made transistors and ICs stable enough to be commercially useful. By 1961, solid-state, discrete op-amps were being produced. These op-amps were effectively small circuit boards with packages such as edge-connectors. They usually had hand-selected resistors in order to improve things such as voltage offset and drift. The P45 (1961) had a gain of 94 dB and ran on ±15 V rails. It was intended to deal with signals in the range of ±10 V.

1962: First op-amps in potted modules

By 1962, several companies were producing modular potted packages that could be plugged into printed circuit boards.[*citation needed*] These packages were crucially important as they made the operational amplifier into a single black box which could be easily treated as a component in a larger circuit.



GAP/R's model PP65: a solid-state op-amp in a potted module (1962).

1963: First monolithic IC op-amp

In 1963, the first monolithic IC op-amp, the μA702 designed by Bob Widlar at Fairchild Semiconductor, was released. Monolithic ICs consist of a single chip as opposed to a chip and discrete parts (a discrete IC) or multiple chips bonded and connected on a circuit board (a hybrid IC). Almost all modern op-amps are monolithic ICs; however, this first IC did not meet with much success. Issues such as an uneven supply voltage, low gain and a small dynamic range held off the dominance of monolithic op-amps until 1965 when the μA709[6] (also designed by Bob Widlar) was released.

1968: Release of the µA741 – would be seen as a nearly ubiquitous chip

The popularity of monolithic op-amps was further improved upon the release of the LM101 in 1967, which solved a variety of issues, and the subsequent release of the µA741 in 1968. The µA741 was extremely similar to the LM101 except that Fairchild's facilities allowed them to include a 30 pF compensation capacitor inside the chip instead of requiring external compensation. This simple difference has made the 741 *the* canonical op-amp and many modern amps base their pinout on the 741s.The µA741 is still in production, and has become ubiquitous in electronics—many manufacturers produce a version of this classic chip, recognizable by part numbers containing *741*.

1966: First varactor bridge op-amps

Since the 741, there have been many different directions taken in op-amp design. Varactor bridge op-amps started to be produced in the late 1960s; they were designed to have extremely small input current and are still amongst the best op-amps available in terms of common-mode rejection with the ability to correctly deal with hundreds of volts at their inputs.

1970: First high-speed, low-input current FET design

In the 1970s high speed, low-input current designs started to be made by using FETs. These would be largely replaced by op-amps made with MOSFETs in the 1980s. During the 1970s single sided supply op-amps also became available.

1972: Single sided supply op-amps being produced

A single sided supply op-amp is one where the input and output voltages can be as low as the negative power supply voltage instead of needing to be at least two volts above it. The result is that it can operate in many applications with the negative supply pin on the op-amp being connected to the signal ground, thus eliminating the need for a separate negative power supply.

The LM324 (released in 1972) was one such op-amp that came in a quad package (four separate op-amps in one package) and became an industry standard. In addition to packaging multiple op-amps in a single package, the 1970s also saw the birth of op-amps in hybrid packages. These op-amps were generally improved versions of existing monolithic op-amps. As the properties of monolithic op-amps improved, the more complex hybrid ICs were quickly relegated to systems that are required to have extremely long service lives or other specialty systems.

Recent trends

Recently supply voltages in analog circuits have decreased (as they have in digital logic) and low-voltage opamps have been introduced reflecting this. Supplies of ±5V and increasingly 5V are common. To maximize the signal range modern op-amps commonly have rail-to-rail inputs (the input signals can range from the lowest supply voltage to the highest) and sometimes rail-to-rail outputs.

Classification of Operational Amplifiers

Op-amps may be classified by their construction:

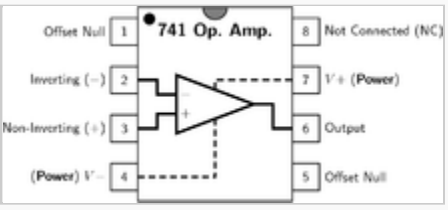
- discrete (built from individual transistors or tubes/valves)
- IC (fabricated in an Integrated circuit) - most common
- hybrid

IC op-amps may be classified in many ways, including:

- Military, Industrial, or Commercial grade (for example: the LM301 is the commercial grade version of the LM101, the LM201 is the industrial version). This may define operating temperature ranges and other environmental or quality factors.
- Classification by package type may also affect environmental hardiness, as well as manufacturing options; DIP, and other through-hole packages are tending to be replaced by Surface-mount devices.
- Classification by internal compensation: op-amps may suffer from high frequency instability in some negative feedback circuits unless a small compensation capacitor modifies the phase- and frequency-responses; op-amps with capacitor built in are termed **compensated**, or perhaps compensated for closed-loop gains down to (say) 5, others: uncompensated.
- Single, dual and quad versions of many commercial op-amp IC are available, meaning 1, 2 or 4 operational amplifiers are included in the same package.
- Rail-to-rail input (and/or output) op-amps can work with input (and/or output) signals very close to the power supply rails.
- CMOS op-amps (such as the CA3140E) provide extremely high input resistances, higher than JFET-input op-amps, which are normally higher than bipolar-input op-amps.
- other varieties of op-amp include programmable op-amps (simply meaning the quiescent current, gain, bandwidth and so on can be adjusted slightly by an external resistor).
- manufacturers often tabulate their op-amps according to purpose, such as low-noise pre-amplifiers, wide bandwidth amplifiers, and so on.

Applications

Main article: Operational amplifier applications



DIP pinout for 741-type operational amplifier

Use in electronics system design

The use of op-amps as circuit blocks is much easier and clearer than specifying all their individual circuit elements (transistors, resistors, etc.), whether the amplifiers used are integrated or discrete. In the first approximation op-amps can be used as if they were ideal differential gain blocks; at a later stage limits can be placed on the acceptable range of parameters for each op-amp.

Circuit design follows the same lines for all electronic circuits. A specification is drawn up governing what the circuit is required to do, with allowable limits. For example, the gain may be required to be 100 times, with a tolerance of 5% but drift of less than 1% in a specified temperature range; the input impedance not less than one megohm; etc.

A basic circuit is designed, often with the help of circuit modeling (on a computer). Specific commercially available op-amps and other components are then chosen that meet the design criteria within the specified tolerances at acceptable cost. If not all criteria can be met, the specification may need to be modified.

A prototype is then built and tested; changes to meet or improve the specification, alter functionality, or reduce the cost, may be made.

Positive feedback configurations

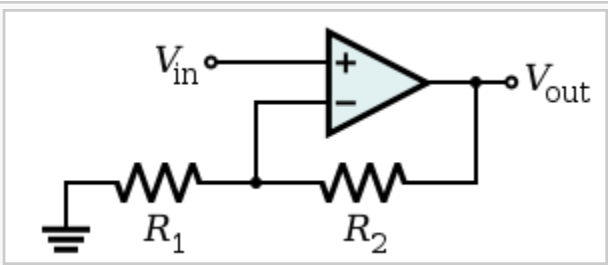
Another typical configuration of op-amps is the positive feedback, which takes a fraction of the output signal back to the non-inverting input. An important application of it is the comparator with hysteresis (i.e., the Schmitt trigger).

Basic single stage amplifiers

Non-inverting amplifier

The gain equation for the op-amp is:

$$V_{\text{out}} = (V_+ - V_-)\, G_{\text{open-loop}}$$



An op-amp connected in the non-inverting amplifier configuration

However, in this circuit V_- is a function of V_{out} because of the negative feedback through the $R_1 R_2$ network. R_1 and R_2 form a voltage divider with reduction factor

$$F = \frac{R_1}{R_1 + R_2}$$

Since the V_- input is a high-impedance input, it does not load the voltage divider appreciably, so:

$$V_- = F \cdot V_{\text{out}}$$

Substituting this into the gain equation, we obtain:

$$V_{\text{out}} = (V_{\text{in}} - F \cdot V_{\text{out}}) \cdot G_{\text{open-loop}}$$

Solving for V_{out}:

$$V_{\text{out}} = V_{\text{in}} \cdot \left(\frac{1}{F + 1/G_{\text{open-loop}}}\right)$$

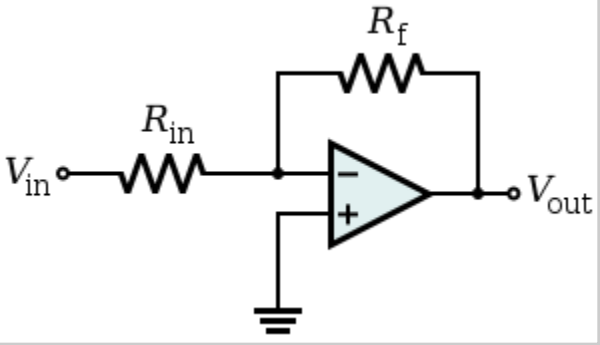
If $G_{\text{open-loop}}$ is very large, this simplifies to

$$V_{out} = \boxed{\frac{V_{\text{in}}}{F}} = V_{\text{in}} / \frac{R_1}{R_1 + R_2} = \boxed{V_{\text{in}}\left(1 + \frac{R_2}{R_1}\right)}.$$

Inverting amplifier

Because it does not require a differential input, this negative feedback connection was the most typical use of an op-amp in the days of analog computers.[*citation needed*] It remains very popular.[*citation needed*]

This circuit is easily analysed with the help of the two "golden rules".



An op-amp connected in the inverting amplifier configuration

Since the non-inverting input is grounded, rule 1 tells us that the inverting input will also be at ground potential (0 Volts):

$$V_- \approx V_+ \ = 0$$

The current through R_{in} is then:

$$I_{in} = V_{\text{in}}/R_{\text{in}}$$

Rule 2 tells us that no current enters the inverting input.
Then, by Kirchoff's current law the current through R_{f} must be the same as the current through R_{in}. The voltage drop across R_{f} is then given by Ohm's law:

$$V_{\text{Rf}} = R_{\text{f}} \cdot I_{\text{in}} = V_{\text{in}} \frac{R_{\text{f}}}{R_{\text{in}}}$$

Since V_- is zero volts, V_{out} is just $-V_{\text{Rf}}$:

$$V_{\text{out}} = -V_{\text{in}} \frac{R_{\text{f}}}{R_{\text{in}}}$$

[7]

- Some Variations:
  - A resistor is often inserted between the non-inverting input and ground (so both inputs "see" similar resistances), reducing the input offset voltage due to different voltage drops due to bias current, and may reduce distortion in some op-amps.
  - A DC-blocking capacitor may be inserted in series with the input resistor when a frequency response down to DC is not needed and any DC voltage on the input is unwanted. That is, the capacitive component of the input impedance inserts a DC zero and a low-frequency pole that gives the circuit a bandpass or high-pass characteristic.

Other applications

- audio- and video-frequency pre-amplifiers and buffers
- voltage comparators
- differential amplifiers
- differentiators and integrators
- filters
- precision rectifiers

- precision peak detectors
- voltage and current regulators
- analog calculators
- analog-to-digital converters
- digital-to-analog converter
- voltage clamps
- oscillators and waveform generators

Most single, dual and quad op-amps available have a standardized pin-out which permits one type to be substituted for another without wiring changes. A specific op-amp may be chosen for its open loop gain, bandwidth, noise performance, input impedance, power consumption, or a compromise between any of these factors.

Limitations of real op-amps

Real op-amps differ from the ideal model in various respects.

IC op-amps as implemented in practice are moderately complex integrated circuits; see the internal circuitry for the relatively simple 741 op-amp below, for example.

DC imperfections

Real operational amplifiers suffer from several non-ideal effects:

Finite gain
: Open-loop gain is infinite in the ideal operational amplifier but finite in real operational amplifiers. Typical devices exhibit open-loop DC gain ranging from 100,000 to over 1 million. So long as the loop gain (i.e., the product of open-loop and feedback gains) is very large, the circuit gain will be determined entirely by the amount of negative feedback (i.e., it will be independent of open-loop gain). In cases where closed-loop gain must be very high, the feedback gain will be very low, and the low feedback gain causes low loop gain; in these cases, the operational amplifier will cease to behave ideally.

Finite input impedance
: The input impedance of the operational amplifier is defined as the impedance *between* its two inputs. It is *not* the impedance from each input to ground. In the typical high-gain negative-feedback applications, the feedback ensures that the two inputs sit at the same voltage, and so the impedance between them is made artificially very high. Hence, this parameter is rarely an important design parameter. Because MOSFET-input operational amplifiers often have protection circuits that effectively short circuit any input differences greater than a small threshold, the input impedance can appear to be very low in some tests. However, as long as these operational amplifiers are used in a typical high-gain negative feedback application, these protection circuits will be inactive and the negative feedback will render the input impedance to be practically infinite. The input bias and leakage currents described below are a more important design parameter for typical operational amplifier applications.

Non-zero output impedance
: Low output impedance is important for low resistance loads; for these loads, the voltage drop across the output impedance of the amplifier will be significant. Hence, the output impedance of the amplifier reflects the maximum power that can be provided. If the output voltage is fed back negatively, the output

impedance of the amplifier is effectively lowered; thus, in linear applications, op-amps usually exhibit a very low output impedance indeed. Negative feedback can not, however, reduce the limitations that R_{load} in conjunction with R_{out} place on the maximum and minimum possible output voltages; it can only reduce output errors *within* that range.

Low-impedance outputs typically require high quiescent (i.e., idle) current in the output stage and will dissipate more power. So low-power designs may purposely sacrifice low-impedance outputs.

Input current

Due to biasing requirements or leakage, a small amount of current (typically ~10 nanoamperes for bipolar op-amps, tens of picoamperes for JFET input stages, and only a few pA for MOSFET input stages) flows into the inputs. When large resistors or sources with high output impedances are used in the circuit, these small currents can produce large unmodeled voltage drops. If the input currents are **matched** *and* the impedance looking *out* of *both* inputs are **matched,** then the voltages produced at each input will be equal. Because the operational amplifier operates on the *difference* between its inputs, these matched voltages will have no effect (unless the operational amplifier has poor CMRR, which is described below). It is more common for the input currents (or the impedances looking out of each input) to be slightly mismatched, and so a small **offset voltage** can be produced. This offset voltage can create offsets or drifting in the operational amplifier. It can often be nulled externally; however, many operational amplifiers include *offset null* or *balance* pins and some procedure for using them to remove this offset. Some operational amplifiers attempt to nullify this offset automatically.

Input offset voltage

This voltage, which is what is required across the op-amp's input terminals to drive the output voltage to zero,[8][nb 1] is related to the mismatches in input bias current. In the perfect amplifier, there would be no input offset voltage. However, it exists in actual op-amps because of imperfections in the differential amplifier that constitutes the input stage of the vast majority of these devices. Input offset voltage creates two problems: First, due to the amplifier's high voltage gain, it virtually assures that the amplifier output will go into saturation if it is operated without negative feedback, even when the input terminals are wired together. Second, in a closed loop, negative feedback configuration, the input offset voltage is amplified along with the signal and this may pose a problem if high precision DC amplification is required or if the input signal is very small.[nb 2]

Common mode gain

A perfect operational amplifier amplifies only the voltage difference between its two inputs, completely rejecting all voltages that are common to both. However, the differential input stage of an operational amplifier is never perfect, leading to the amplification of these identical voltages to some degree. The standard measure of this defect is called the common-mode rejection ratio (denoted CMRR). Minimization of common mode gain is usually important in non-inverting amplifiers (described below) that operate at high amplification.

Temperature effects

All parameters change with temperature. Temperature drift of the input offset voltage is especially important.

Power-supply rejection

The output of a perfect operational amplifier will be completely independent from ripples that arrive on its power supply inputs. Every real operational amplifier has a specified power supply rejection ratio (PSRR) that reflects how well the op-amp can reject changes in its supply voltage. Copious use of bypass

capacitors can improve the PSRR of many devices, including the operational amplifier.

Drift

Real op-amp parameters are subject to slow change over time and with changes in temperature, input conditions, etc.

AC imperfections

The op-amp gain calculated at DC does not apply at higher frequencies. To a first approximation, the gain of a typical op-amp is inversely proportional to frequency. This means that an op-amp is characterized by its gain-bandwidth product. For example, an op-amp with a gain bandwidth product of 1 MHz would have a gain of 5 at 200 kHz, and a gain of 1 at 1 MHz. This low-pass characteristic is introduced deliberately, because it tends to stabilize the circuit by introducing a dominant pole. This is known as frequency compensation.

Typical low cost, general purpose op-amps exhibit a gain bandwidth product of a few megahertz. Specialty and high speed op-amps can achieve gain bandwidth products of hundreds of megahertz. For very high-frequency circuits, a completely different form of op-amp called the current-feedback operational amplifier is often used.

Other imperfections include:

- Finite bandwidth — all amplifiers have a finite bandwidth. This creates several problems for op amps. First, associated with the bandwidth limitation is a phase difference between the input signal and the amplifier output that can lead to oscillation in some feedback circuits. The internal frequency compensation used in some op amps to increase the gain or phase margin intentionally reduces the bandwidth even further to maintain output stability when using a wide variety of feedback networks. Second, reduced bandwidth results in lower amounts of feedback at higher frequencies, producing higher distortion, noise, and output impedance and also reduced output phase linearity as the frequency increases.
- Input capacitance — most important for high frequency operation because it further reduces the open loop bandwidth of the amplifier.
- Common mode gain — See DC imperfections, above.

Nonlinear imperfections

- Saturation — output voltage is limited to a minimum and maximum value close to the power supply voltages.[nb 3] Saturation occurs when the output of the amplifier reaches this value and is usually due to:
  - In the case of an op-amp using a bipolar power supply, a voltage gain that produces an output that is more positive or more negative than that maximum or minimum; or
  - In the case of an op-amp using a single supply voltage, either a voltage gain that produces an output that is more positive than that maximum, or a signal so close to ground that the amplifier's gain is not sufficient to raise it above the lower threshold.[nb 4]
- Slewing — the amplifier's output voltage reaches its maximum rate of change. Measured as the slew rate, it is usually specified in volts per microsecond. When slewing occurs, further increases in the input signal have no effect on the rate of change of the output. Slewing is usually caused by internal capacitances in the amplifier, especially those used to implement its frequency compensation.
- Non-linear transfer function — The output voltage may not be accurately proportional to the difference between the input voltages. It is commonly called distortion when the input signal is a waveform. This

effect will be very small in a practical circuit if substantial negative feedback is used.

Power considerations

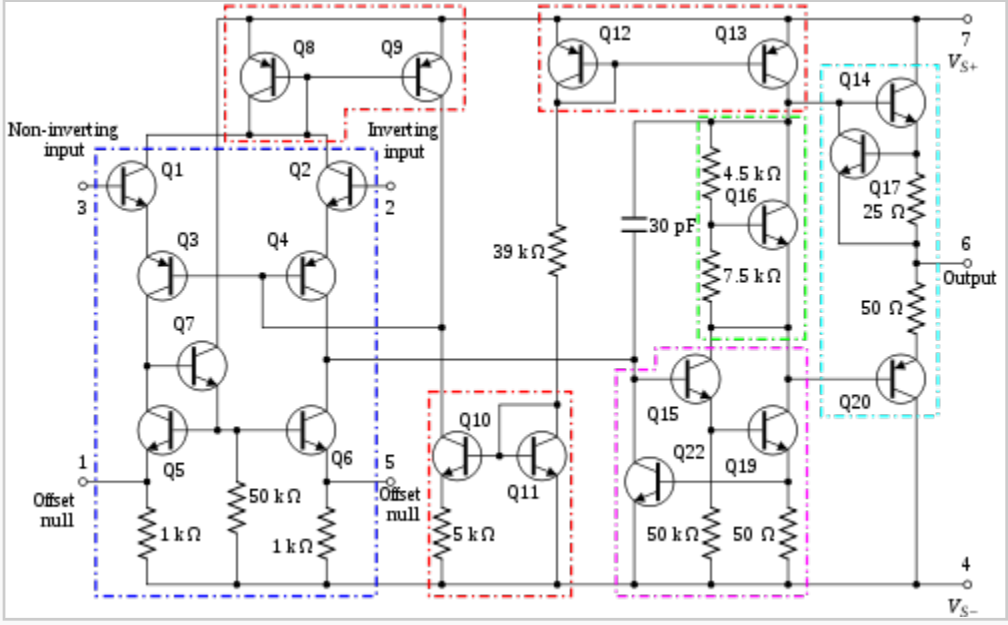
- Limited output current — the output current must obviously be finite. In practice, most op-amps are designed to limit the output current so as not to exceed a specified level — around 25 mA for a type 741 IC op-amp — thus protecting the op-amp and associated circuitry from damage. Modern designs are electronically more rugged than earlier implementations and some can sustain direct short circuits on their outputs without damage.
- Limited dissipated power — an op-amp is a linear amplifier. It therefore dissipates some power as heat, proportional to the output current, and to the difference between the output voltage and the supply voltage. If the op-amp dissipates too much power, then its temperature will increase above some safe limit. The op-amp may enter thermal shutdown, or it may be destroyed.

Modern integrated FET or MOSFET op-amps approximate more closely the ideal op-amp than bipolar ICs when it comes to input impedance and input bias and offset currents. Bipolars are generally better when it comes to input *voltage* offset, and often have lower noise. Generally, at room temperature, with a fairly large signal, and limited bandwidth, FET and MOSFET op-amps now offer better performance.

Internal circuitry of 741 type op-amp

Though designs vary between products and manufacturers, all op-amps have basically the same internal structure, which consists of three stages:

1. Differential amplifier – provides low noise amplification, high input impedance, usually a differential output.
2. Voltage amplifier – provides high voltage gain, a single-pole frequency roll-off, usually single-ended output.
3. Output amplifier – provides high current driving capability, low output impedance, current limiting and short circuit protection circuitry.



A component level diagram of the common 741 op-amp. Dotted lines outline: current mirrors (red); differential amplifier (blue); class A gain stage (magenta); voltage level shifter (green); output stage (cyan).

Input stage

Constant-current stabilization system

The input stage DC conditions are stabilized by a high-gain negative feedback system whose main parts are the two current mirrors on the left of the figure, outlined in red. The main purpose of this negative feedback system—to supply the differential input stage with a stable constant current—is realized as follows.

The current through the 39 kΩ resistor acts as a current reference for the other bias currents used in the chip. The voltage across the resistor is equal to the voltage across the supply rails ($V_{S+} - V_{S-}$) minus two transistor diode drops (i.e., from Q11 and Q12), and so the current has value $I_{\text{ref}} = (V_{S+} - V_{S-} - 2V_{be})/(39\ \text{k}\Omega)$. The Widlar current mirror built by Q10, Q11, and the 5 kΩ resistor produces a very small fraction of I_{ref} at the Q10 collector. This small constant current through Q10's collector supplies the base currents for Q3 and Q4 as well as the Q9 collector current. The Q8/Q9 current mirror tries to make Q9's collector current the same as the Q3 and Q4 *collector* currents. Thus Q3 and Q4's combined base currents (which are of the same order as the overall chip's input currents) will be a small fraction of the already small Q10 current.

So, if the input stage current increases for any reason, the Q8/Q9 current mirror will draw current away from the bases of Q3 and Q4, which reduces the input stage current, and vice versa. The feedback loop also isolates the rest of the circuit from common-mode signals by making the base voltage of Q3/Q4 follow tightly $2V_{be}$ below the higher of the two input voltages.

Differential amplifier

The blue outlined section is a differential amplifier. Q1 and Q2 are input emitter followers and together with the common base pair Q3 and Q4 form the differential input stage. In addition, Q3 and Q4 also act as level shifters and provide voltage gain to drive the class A amplifier. They also help to increase the reverse V_{be} rating on the input transistors (the emitter-base junctions of the NPN transistors Q1 and Q2 break down at around 7 V but the PNP transistors Q3 and Q4 have breakdown voltages around 50 V)[9].

The differential amplifier formed by Q1–Q4 drives a current mirror active load formed by transistors Q5–Q7 (actually, Q6 is the very active load). Q7 increases the accuracy of the current mirror by decreasing the amount of signal current required from Q3 to drive the bases of Q5 and Q6. This configuration provides differential to single ended conversion as follows:

The signal current of Q3 is the input to the current mirror while the output of the mirror (the collector of Q6) is connected to the collector of Q4. Here, the signal currents of Q3 and Q4 are summed. For differential input signals, the signal currents of Q3 and Q4 are equal and opposite. Thus, the sum is twice the individual signal currents. This completes the differential to single ended conversion.

The open circuit signal voltage appearing at this point is given by the product of the summed signal currents and the paralleled collector resistances of Q4 and Q6. Since the collectors of Q4 and Q6 appear as high resistances to the signal current, the open circuit voltage gain of this stage is very high.

It should be noted that the base current at the inputs is not zero and the effective (differential) input impedance of a 741 is about 2 MΩ. The "offset null" pins may be used to place external resistors in parallel with the two 1 kΩ resistors (typically in the form of the two ends of a potentiometer) to adjust the balancing of the Q5/Q6 current mirror and thus indirectly control the output of the op-amp when zero signal is applied between the inputs.

Class A gain stage

The section outlined in magenta is the class A gain stage. The top-right current mirror Q12/Q13 supplies this stage by a constant current load, via the collector of Q13, that is largely independent of the output voltage. The stage consists of two NPN transistors in a Darlington configuration and uses the output side of a current mirror as its collector load to achieve high gain. The 30 pF capacitor provides frequency selective negative feedback around the class A gain stage as a means of frequency compensation to stabilise the amplifier in feedback configurations. This technique is called Miller compensation and functions in a similar manner to an op-amp integrator circuit. It is also known as 'dominant pole compensation' because it introduces a dominant pole (one which masks the effects of other poles) into the open loop frequency response. This pole can be as low as 10 Hz in a 741 amplifier and it introduces a −3 dB loss into the open loop response at this frequency. This internal compensation is provided to achieve unconditional stability of the amplifier in negative feedback configurations where the feedback network is non-reactive and the closed loop gain is unity or higher. Hence, the use of the operational amplifier is simplified because no external compensation is required for unity gain stability; amplifiers without this internal compensation may require external compensation or closed loop gains significantly higher than unity.

Output bias circuitry

The green outlined section (based around Q16) is a voltage level shifter or rubber diode (i.e., a V_{BE} multiplier); a type of voltage source. In the circuit as shown, Q16 provides a constant voltage drop between its collector and emitter regardless of the current through the circuit. If the base current to the transistor is assumed to be zero, and the voltage between base and emitter (and across the 7.5 kΩ resistor) is 0.625 V (a typical value for a BJT in the active region), then the current through the 4.5 kΩ resistor will be the same as that through the 7.5 kΩ, and will produce a voltage of 0.375 V across it. This keeps the voltage across the transistor, and the two resistors at 0.625 + 0.375 = 1 V. This serves to bias the two output transistors slightly into conduction reducing crossover distortion. In some discrete component amplifiers this function is achieved with (usually two) silicon diodes.

Output stage

The output stage (outlined in cyan) is a Class AB push-pull emitter follower (Q14, Q20) amplifier with the bias set by the V_{be} multiplier voltage source Q16 and its base resistors. This stage is effectively driven by the collectors of Q13 and Q19. Variations in the bias with temperature, or between parts with the same type number, are common so crossover distortion and quiescent current may be subject to significant variation. The output range of the amplifier is about one volt less than the supply voltage, owing in part to V_{be} of the output transistors Q14 and Q20.

The 25 Ω resistor in the output stage acts as a current sense to provide the output current-limiting function which limits the current in the emitter follower Q14 to about 25 mA for the 741. Current limiting for the negative output is done by sensing the voltage across Q19's emitter resistor and using this to reduce the drive into Q15's base. Later versions of this amplifier schematic may show a slightly different method of output current limiting. The output resistance is not zero, as it would be in an ideal op-amp, but with negative feedback it approaches zero at low frequencies.

Note: while the 741 was historically used in audio and other sensitive equipment, such use is now rare because of the improved noise performance of more modern op-amps. Apart from generating noticeable hiss, 741s and other older op-amps may have poor common-mode rejection ratios and so will often introduce cable-borne mains hum and other common-mode interference, such as switch 'clicks', into sensitive equipment.

The "741" has come to often mean a generic op-amp IC (such as uA741, LM301, 558, LM324, TBA221 - or a more modern replacement such as the TL071). The description of the 741 output stage is qualitatively similar for many other designs (that may have quite different input stages), except:

- Some devices (uA748, LM301, LM308) are not internally compensated (require an external capacitor from output to some point within the operational amplifier, if used in low closed-loop gain applications).
- Some modern devices have rail-to-rail output capability (output can be taken to positive or negative power supply rail within a few millivolts).

See also

- Operational amplifier applications
- Differential amplifier
- Instrumentation amplifier
- Active filter
- Current-feedback operational amplifier
- Operational transconductance amplifier
- George A. Philbrick
- Analog computer
- Negative feedback amplifier

Notes

1. ^ This definition hews to the convention of measuring op-amp parameters with respect to the zero voltage point in the circuit, which is usually half the total voltage between the amplifier's positive and negative power rails.
2. ^ Many older designs of operational amplifiers have offset null inputs to allow the offset to be manually adjusted away. Modern precision op-amps can have internal circuits that automatically cancel this offset using choppers or other circuits that measure the offset voltage periodically and subtract it from the input voltage.
3. ^ That the output cannot reach the power supply voltages is usually the result of limitations of the amplifier's output stage transistors. See "Output stage," below.
4. ^ The output of older op-amps can reach to within one or two volts of the supply rails. The output of newer so-called "rail to rail" op-amps can reach to within millivolts of the supply rails when providing low output currents.

References

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2. ^ Paul Horowitz and Winfield Hill, *The Art of Electronics*, Cambridge University Press, 1989, p 177.
3. ^ Jung, Walter G. (2004). "Chapter 8: Op Amp History" (http://books.google.com/books?id=dunqt1rt4sAC) . *Op Amp Applications Handbook*. Newnes. p. 777. ISBN 9780750678445. http://books.google.com/books?id=dunqt1rt4sAC. Retrieved 2008-11-15.
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5. ^ http://www.analog.com/library/analogDialogue/archives/39-05/Web_ChH_final.pdf

6. ^ A.P. Malvino, *Electronic Principles* (2nd Ed. 1979. ISBN 0-07-039867-4) p. 476.
7. ^ Electronic Circuits (Fifth edition) by Sedra/Smith
8. ^ D.F. Stout *Handbook of Operational Amplifier Circuit Design* (McGraw-Hill, 1976, ISBN 007061797X) pp. 1–11.
9. ^ The uA741 Operational Amplifier (http://ecow.engr.wisc.edu/cgi-bin/get/ece/342/schowalter/notes/chapter10/theua741operationalamplifier.ppt)

External links

- Introduction to op-amp circuit stages, second order filters, single op-amp bandpass filters, and a simple intercom (http://www.bowdenshobbycircuits.info/opamp.htm)
- Hyperphysics – descriptions of common applications (http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/opampvar.html)
- Single supply op-amp circuit collection (http://instruct1.cit.cornell.edu/courses/bionb440/datasheets/SingleSupply.pdf)
- Op-amp circuit collection (http://www.national.com/an/AN/AN-31.pdf)
- Another introduction (http://web.telia.com/~u85920178/begin/opamp00.htm)
- Op-Amp Handbook (http://www.engineering.uiowa.edu/~bme080/supplementary_info/BBTI_AppCkts.pdf)
- Opamps for everyone (http://focus.ti.com/lit/an/slod006b/slod006b.pdf) Downloadable book.
- *MOS op amp design: A tutorial overview* (http://www.ee.unb.ca/Courses/EE3122/DFL/AdditionalMaterial/OpAmps/MOS_OpAmpTutorial.pdf)
- *High Speed OpAmp Techniques* (http://cds.linear.com/docs/Application%20Note/an47fa.pdf) very practical and readable - with photos and real waveforms
- Op Amp Applications (http://www.analog.com/library/analogDialogue/archives/39-05/op_amp_applications_handbook.html) Downloadable book. Can also be bought
- Operational Amplifier Noise Prediction (All Op Amps) (http://www.intersil.com/data/an/an519.pdf) using spot noise
- Operational Amplifier Basics (http://www.williamson-labs.com/480_opam.htm)
- History of the Op-amp (http://www.analog.com/library/analogDialogue/archives/39-05/Web_ChH_final.pdf) from vacuum tubes to about 2002. Lots of detail, with schematics. IC part is somewhat ADI-centric.
- IC Op-Amps Through the Ages (http://www.calvin.edu/~pribeiro/courses/engr332/Handouts/ho18opamp.pdf)
- ECE 209: Operational amplifier basics (http://www.tedpavlic.com/teaching/osu/ece209/support/opamp_basics.pdf) – Brief document explaining zero error by naive high-gain negative feedback. Gives single OpAmp example that generalizes typical configurations.

Retrieved from "http://en.wikipedia.org/wiki/Operational_amplifier"
Categories: Electronic amplifiers | Integrated circuits

Operational amplifier applications

From Wikipedia, the free encyclopedia

This article illustrates some typical **applications** of **operational amplifiers**. A simplified schematic notation is used, and the reader is reminded that many details such as device selection and power supply connections are not shown.

Contents

Practical circuits

It is important to note that the equations shown below, pertaining to each type of circuit, assume that an ideal op amp is used. Those interested in construction of any of these circuits for practical use should consult a more detailed reference. See the External links and Further reading sections.

Resistors used in practical solid-state op-amp circuits are typically in the kΩ range. Resistors much greater than 1 MΩ cause excessive thermal noise and make the circuit operation susceptible to significant errors due to bias or leakage currents.

Practical operational amplifiers draw a small current from each of their inputs due to bias requirements and leakage. These currents flow through the resistances connected to the inputs and produce small voltage drops across those resistances. In AC signal applications this seldom matters. If high-precision DC operation is required, however, these voltage drops need to be considered. The design technique is to try to ensure that these voltage drops are equal for both inputs, and therefore cancel. If these voltage drops are equal and the common-mode rejection ratio of the operational amplifier is good, there will be considerable cancellation and improvement in DC accuracy.

If the input currents into the operational amplifier are equal, to reduce offset voltage the designer must ensure that the DC resistance looking out of each input is also matched. In general input currents differ, the difference being called the *input offset current*, I_{os}. Matched external input resistances R_{in} will still produce an input voltage error of $R_{in} \cdot I_{os}$. Most manufacturers provide a method for tuning the operational amplifier to balance the input currents (e.g., "offset null" or "balance" pins that can interact with an external voltage source attached to a potentiometer). Otherwise, a tunable external voltage can be added to one of the inputs in order to balance out the offset effect. In cases where a design calls for one input to be short-circuited to ground, that short circuit can be replaced with a variable resistance that can be tuned to mitigate the offset problem.

Note that many operational amplifiers that have MOSFET-based input stages have input leakage currents that will truly be negligible to most designs.

Power supply effects

Although the power supplies are not shown in the operational amplifier designs below, they can be critical in operational amplifier design.

Power supply imperfections (e.g., power signal ripple, non-zero source impedance) may lead to noticeable deviations from ideal operational amplifier behavior. For example, operational amplifiers have a specified power supply rejection ratio that indicates how well the output can reject signals that appear on the power supply inputs. Power supply inputs are often noisy in large designs because the power supply is used by nearly every component in the design, and inductance effects prevent current from being instantaneously delivered to every component at once. As a consequence, when a component requires large injections of current (e.g., a digital component that is frequently switching from one state to another), nearby components can experience sagging at their connection to the power supply. This problem can be mitigated with copious use of bypass capacitors placed connected across each power supply pin and ground. When bursts of current are required by a component, the component can *bypass* the power supply by receiving the current directly from the nearby capacitor (which is then slowly charged by the power supply).

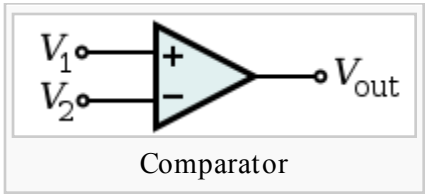
Additionally, current drawn into the operational amplifier from the power supply can be used as inputs to

external circuitry that augment the capabilities of the operational amplifier. For example, an operational amplifier may not be fit for a particular high-gain application because its output would be required to generate signals outside of the safe range generated by the amplifier. In this case, an external push–pull amplifier can be controlled by the current into and out of the operational amplifier. Thus, the operational amplifier may itself operate within its factory specified bounds while still allowing the negative feedback path to include a large output signal well outside of those bounds.[1]

Linear circuit applications

Comparator

Main article: Comparator



Comparator

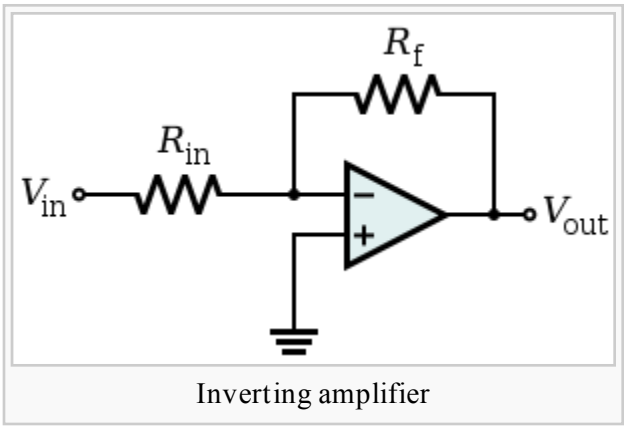
Compares two voltages and switches its output to indicate which voltage is larger.

- $V_{out} = \begin{cases} V_{S+} & V_1 > V_2 \\ V_{S-} & V_1 < V_2 \end{cases}$

(where V_S is the supply voltage and the opamp is powered by $+V_S$ and $-V_S$.)

Inverting amplifier

An inverting amplifier uses negative feedback to invert and amplify a voltage. The R_f resistor allows some of the output signal to be returned to the input. Since the output is 180° out of phase, this amount is effectively subtracted from the input, thereby reducing the input into the operational amplifier. This reduces the overall gain of the amplifier and is dubbed negative feedback.[2]



Inverting amplifier

$$V_{out} = -\frac{R_f}{R_{in}} V_{in}$$

- $Z_{in} = R_{in}$ (because $V-$ is a virtual ground)
- A third resistor, of value $R_f \| R_{in} \triangleq R_f R_{in} / (R_f + R_{in})$, added between the non-inverting input and ground, while not necessary, minimizes errors due to input bias currents.

[3]

The gain of the amplifier is determined by the ratio of R_f to R_{in}. That is:

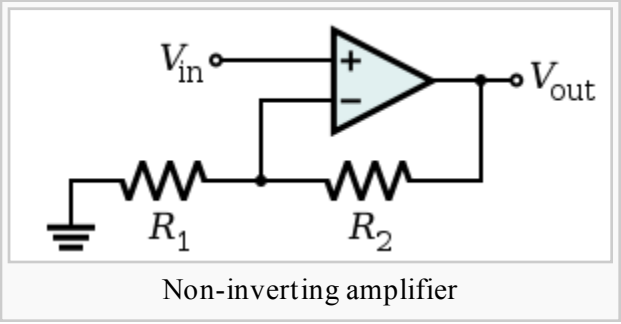
$$A = -\frac{R_f}{R_{in}}$$

The presence of the negative sign is a convention indicating that the output is inverted. For example, if R_f is 10,000 Ω and R_{in} is 1,000 Ω, then the gain would be -10000Ω/1000Ω, which is -10. [4]

Non-inverting amplifier

Amplifies a voltage (multiplies by a constant greater than 1)

$$V_{\text{out}} = V_{\text{in}} \left(1 + \frac{R_2}{R_1}\right)$$



Non-inverting amplifier

- Input impedance $Z_{\text{in}} \approx \infty$
  - The input impedance is *at least* the impedance between non-inverting ($+$) and inverting ($-$) inputs, which is typically 1 MΩ to 10 TΩ, plus the impedance of the path from the inverting ($-$) input to ground (i.e., R_1 in parallel with R_2).
  - Because negative feedback ensures that the non-inverting and inverting inputs match, the input impedance is actually **much higher.**
- Although this circuit has a large input impedance, it suffers from error of input bias current.
  - The non-inverting ($+$) and inverting ($-$) inputs draw small leakage currents into the operational amplifier.
  - These input currents generate voltages that act like unmodeled input offsets. These unmodeled effects can lead to noise on the output (e.g., offsets or drift).
  - Assuming that the two leaking currents are **matched,** their effect can be mitigated by ensuring the DC impedance looking **out** of each input is the same.
    - The voltage produced by each bias current is equal to the product of the bias current with the equivalent DC impedance looking out of each input. Making those impedances equal makes the offset voltage at each input equal, and so the non-zero bias currents will have no impact on the **difference** between the two inputs.
    - A resistor of value

      $$R_1 \| R_2 \triangleq \left(\frac{1}{R_1} + \frac{1}{R_2}\right)^{-1} = \frac{R_1 R_2}{R_1 + R_2},$$

      which is the equivalent resistance of R_1 in parallel with R_2, between the V_{in} source and the non-inverting ($+$) input will ensure the impedances looking **out** of each input will be matched.
    - The matched bias currents will then generate matched offset voltages, and their effect will be hidden to the operational amplifier (which acts on the difference between its inputs) so long as the CMRR is good.
  - Very often, the input currents are *not* matched.
    - Most operational amplifiers provide some method of balancing the two input currents (e.g., by way of an external potentiometer).
    - Alternatively, an external offset can be added to the operational amplifier input to nullify the effect.

- Another solution is to insert a variable resistor between the V_{in} source and the non-inverting ($+$) input. The resistance can be tuned until the offset voltages at each input are matched.
- Operational amplifiers with MOSFET-based input stages have input currents that are so small that they often can be neglected.

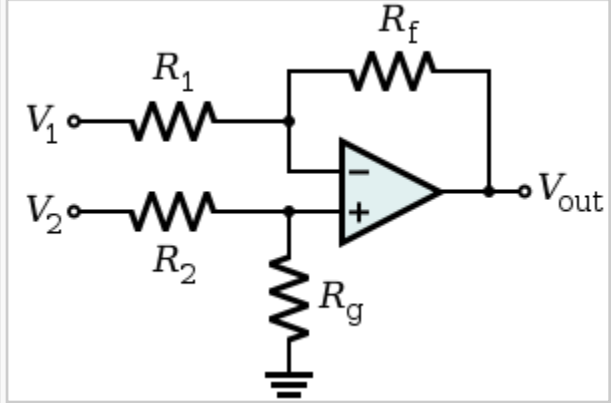
Differential amplifier

Main article: Differential amplifier

The circuit shown is used for finding the difference of two voltages each multiplied by some constant (determined by the resistors).

The name "differential amplifier" should not be confused with the "differentiator", also shown on this page.

$$V_{\text{out}} = \frac{(R_{\text{f}} + R_1)\,R_{\text{g}}}{(R_{\text{g}} + R_2)\,R_1} V_2 - \frac{R_{\text{f}}}{R_1} V_1$$



Differential amplifier

- Differential Z_{in} (between the two input pins) = $R_1 + R_2$ (Note: this is approximate)

For common-mode rejection, anything done to one input must be done to the other. The addition of a compensation capacitor in parallel with Rf, for instance, must be balanced by an equivalent capacitor in parallel with Rg.

The "instrumentation amplifier", which is also shown on this page, is another form of differential amplifier that also provides high input impedance.

Amplified difference

Whenever $R_1 = R_2$ and $R_{\text{f}} = R_{\text{g}}$,

$$V_{\text{out}} = A(V_2 - V_1) \quad \text{and} \quad A \triangleq \frac{R_{\text{f}}}{R_1}$$

Difference amplifier

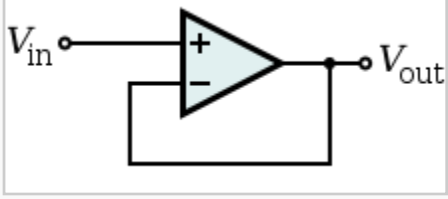
When $R_1 = R_{\text{f}}$ and $R_2 = R_{\text{g}}$:

$$V_{\text{out}} = V_2 - V_1$$

Voltage follower

Used as a buffer amplifier to eliminate loading effects (e.g., connecting a device with a high source impedance to a device with a low input impedance).

$V_{\text{out}} = V_{\text{in}}$
$Z_{\text{in}} = \infty$ (realistically, the differential input impedance of the op-amp itself, 1 MΩ to 1 TΩ)



Voltage follower

Due to the strong (i.e., unity gain) feedback and certain non-ideal characteristics of real operational amplifiers, this feedback system is prone to have poor stability margins. Consequently, the system may be unstable when connected to sufficiently capacitive loads. In these cases, a lag compensation network (e.g., connecting the load to the voltage follower through a resistor) can be used to restore stability. The manufacturer data sheet for the operational amplifier may provide guidance for the selection of components in external compensation networks. Alternatively, another operational amplifier can be chosen that has more appropriate internal compensation.

Summing amplifier

A summing amplifer sums several (weighted) voltages:

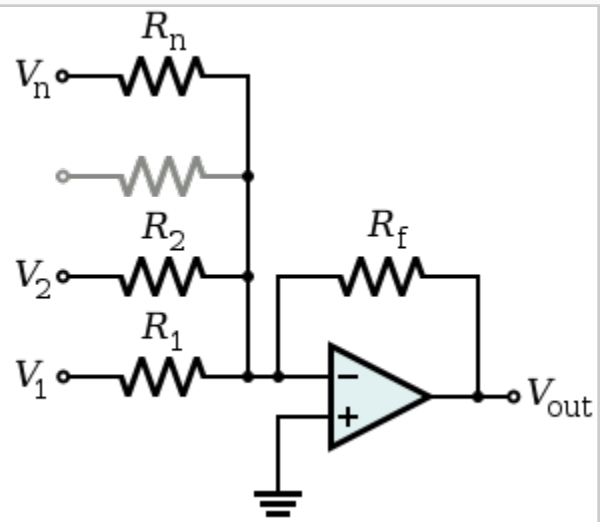
$$V_{\text{out}} = -R_{\text{f}} \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \cdots + \frac{V_n}{R_n} \right)$$

- When $R_1 = R_2 = \cdots = R_n$, and R_{f} independent

$$V_{\text{out}} = -\frac{R_{\text{f}}}{R_1}(V_1 + V_2 + \cdots + V_n)$$

- When $R_1 = R_2 = \cdots = R_n = R_{\text{f}}$

$$V_{\text{out}} = -(V_1 + V_2 + \cdots + V_n)$$



Summing amplifier

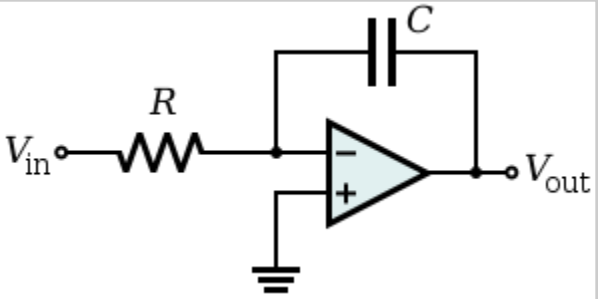
- Output is inverted
- Input impedance of the ***n*th** input is $Z_n = R_n$ ($V-$ is a virtual ground)

Integrator

Integrates the (inverted) signal over time

$$V_{\text{out}} = -\int_0^t \frac{V_{\text{in}}}{RC}\,\mathrm{d}t + V_{\text{initial}}$$

(where V_{in} and V_{out} are functions of time, V_{initial} is the output voltage of the integrator at time $t = 0$.)



Integrating amplifier

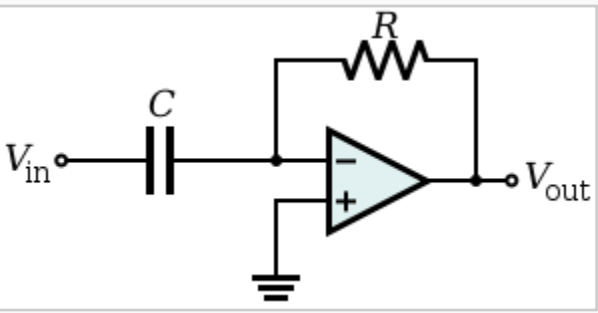
- Note that this can also be viewed as a low-pass electronic filter. It is a filter with a single pole at DC (i.e., where $\omega = 0$) and gain.
- There are several potential problems with this circuit.
  - It is usually assumed that the input V_{in} has zero DC component (i.e., has a zero average value). Otherwise, unless the capacitor is periodically discharged, the output will drift outside of the operational amplifier's operating range.
  - Even when V_{in} has no offset, the leakage or bias currents into the operational amplifier inputs can add an unexpected offset voltage to V_{in} that causes the output to drift. Balancing input currents **and** replacing the non-inverting ($+$) short-circuit to ground with a resistor with resistance R can reduce the severity of this problem.
  - Because this circuit provides no DC feedback (i.e., the capacitor appears like an open circuit to signals with $\omega = 0$), the offset of the output may not agree with expectations (i.e., V_{initial} may be out of the designer's control with the present circuit).

Many of these problems can be made less severe by adding a *large* resistor R_F in parallel with the feedback capacitor. At significantly high frequencies, this resistor will have negligible effect. However, at low frequencies where there are drift and offset problems, the resistor provides the necessary feedback to hold the output steady at the correct value. In effect, this resistor reduces the DC gain of the "integrator" – it goes from infinite to some finite value R_F / R.

Differentiator

Differentiates the (inverted) signal over time.

The name "differentiator" should not be confused with the "differential amplifier," which is also shown on this page. The former takes a derivative and the latter takes a difference (i.e., does subtraction). This is a circuit that could be used in an analog computer, but in practice these circuits are difficult to keep stable and noise-free, so often the problem can be rearranged to use an integrator instead.



Differentiating amplifier

$$V_{\text{out}} = -RC\,\frac{\mathrm{d}V_{\text{in}}}{\mathrm{d}t} \qquad \text{where } V_{\text{in}} \text{ and } V_{\text{out}} \text{ are functions of time.}$$

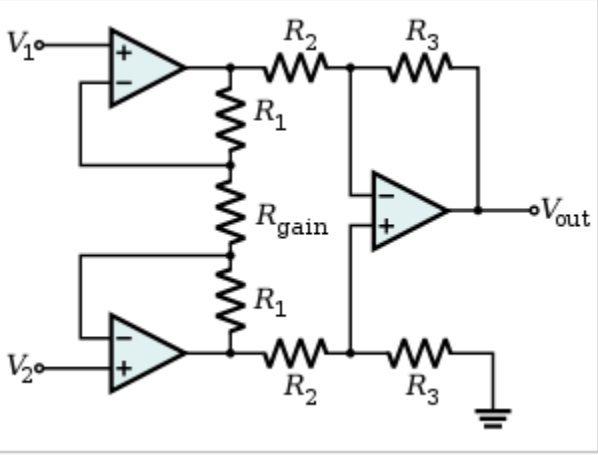
- Note that this can also be viewed as a high-pass electronic filter. It is a filter with a single zero at DC (i.e., where $\omega = 0$) and gain.

Instrumentation amplifier

Main article: Instrumentation amplifier

Combines very high input impedance, high common-mode rejection, low DC offset, and other properties used in making very accurate, low-noise measurements

- Is made by adding a non-inverting buffer to each input of the differential amplifier to increase the input impedance.



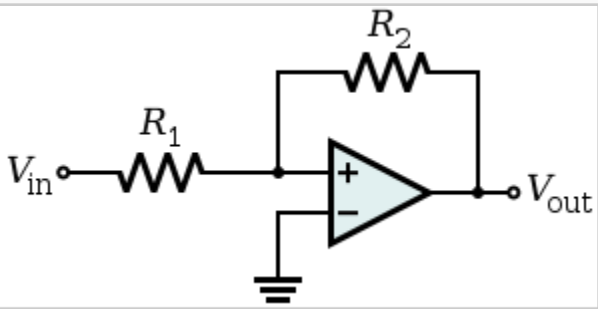
Instrumentation amplifier

Schmitt trigger

Main article: Schmitt trigger

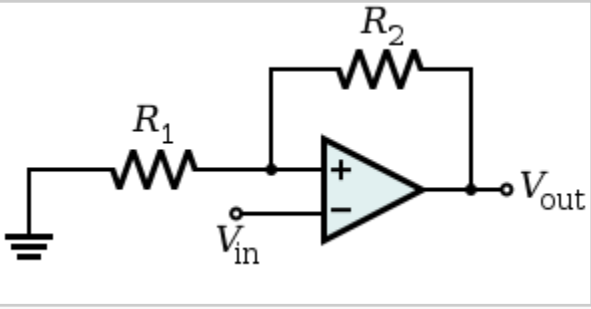
A bistable multivibrator implemented as a comparator with hysteresis.

In this configuration, the hysteresis curve is non-inverting (i.e., very negative inputs correspond to a negative output and very positive inputs correspond to a positive output), and the switching thresholds are $\pm\frac{R_1}{R_2}V_{\text{sat}}$ where V_{sat} is the greatest output magnitude of the operational amplifier.



Schmitt trigger with non-inverting hysteretic switching characteristic

Alternatively, the input and the ground may be swapped. In this configuration, the hysteresis curve is inverting (i.e., very negative inputs correspond to a positive output and vice versa), and the switching thresholds are $\pm\frac{R_1}{R_1+R_2}V_{\mathbf{sat}}$. Such a configuration is used in the relaxation oscillator shown below.

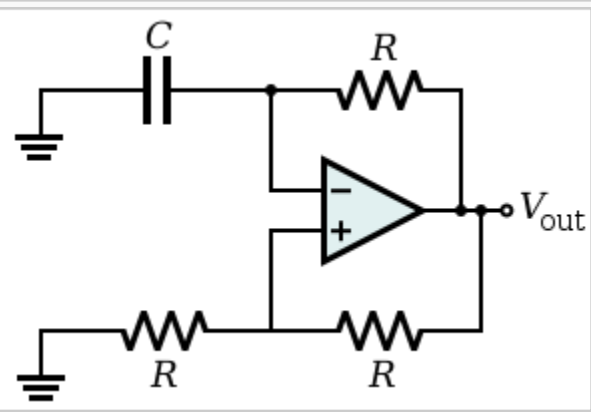


Schmitt trigger with inverting hysteretic switching characteristic

Relaxation oscillator

Main article: Relaxation oscillator

By using an RC network to add slow negative feedback to the inverting Schmitt trigger, a relaxation oscillator is formed. The feedback through the RC network causes the Schmitt trigger output to oscillate in an endless symmetric square wave (i.e., the Schmitt trigger in this configuration is an astable multivibrator).

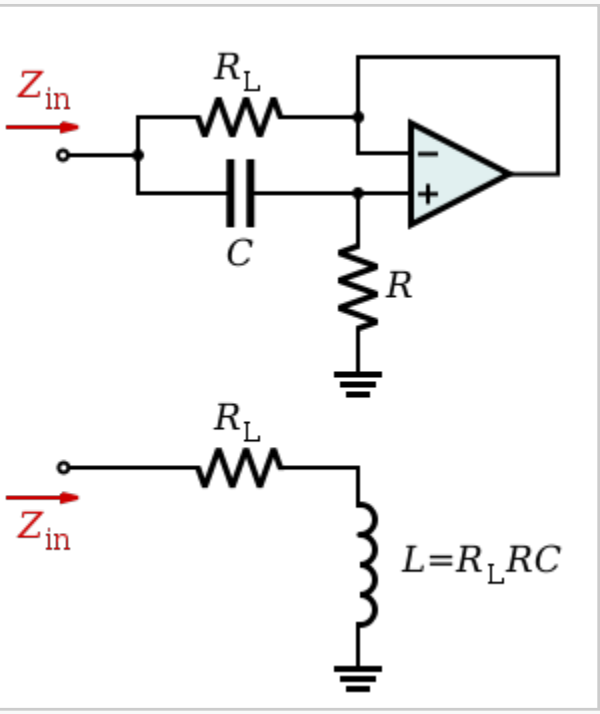


Relaxation oscillator implemented with inverting Schmitt trigger and RC network

Inductance gyrator

Main article: Gyrator

Simulates an inductor (i.e., provides inductance without the use of a possibly costly inductor).



Inductance gyrator

Zero level detector

Voltage divider reference

- Zener sets reference voltage

Negative impedance converter (NIC)

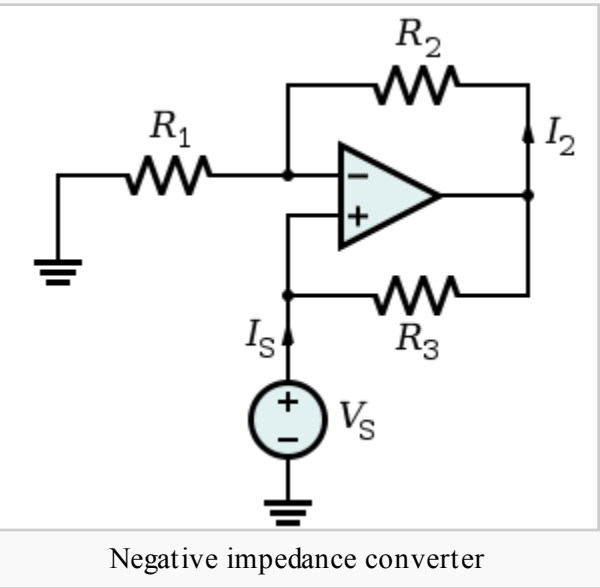
Main article: Negative impedance converter

Creates a resistor having a negative value for any signal generator

- In this case, the ratio between the input voltage and the input current (thus the input resistance) is given by:

$$R_{\text{in}} = -R_3 \frac{R_1}{R_2}$$

In general, the components R_1, R_2, and R_3 need not be resistors; they can be any component that can be described with an impedance.

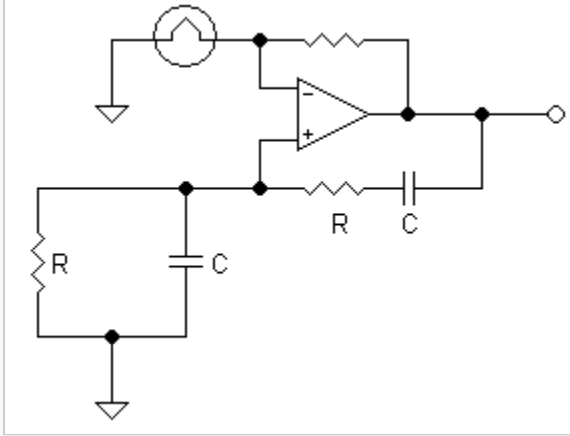


Negative impedance converter

Wien bridge oscillator

Main article: Wien bridge oscillator

Produces a pure sine wave.



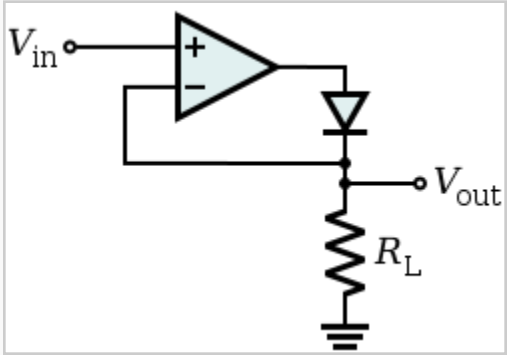
Wien bridge oscillator

Non-linear configurations

Precision rectifier

Main article: Precision rectifier

Although there are some limitations, this **super diode** circuit behaves like an ideal diode for the load R_{L}.



Precision rectifier

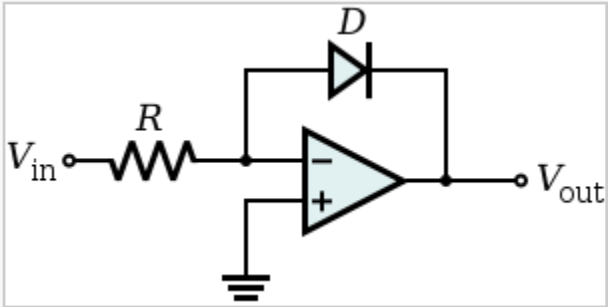
Logarithmic output

See also: Log amplifier

- The relationship between the input voltage v_{in} and the output voltage v_{out} is given by:

$$v_{\mathrm{out}} = -V_{\mathrm{T}} \ln\left(\frac{v_{\mathrm{in}}}{I_{\mathrm{S}} R}\right)$$

  where I_{S} is the *saturation current* and V_{T} is the *thermal voltage*.



Logarithmic configuration

- If the operational amplifier is considered ideal, the negative pin is virtually grounded, so the current flowing into the resistor from the source (and thus through the diode to the output, since the op-amp inputs draw no current) is:

$$\frac{v_{\text{in}}}{R} = I_{\text{R}} = I_{\text{D}}$$

where I_{D} is the current through the diode. As known, the relationship between the current and the voltage for a diode is:

$$I_{\text{D}} = I_{\text{S}} \left(e^{\frac{V_{\text{D}}}{V_{\text{T}}}} - 1 \right).$$

This, when the voltage is greater than zero, can be approximated by:

$$I_{\text{D}} \simeq I_{\text{S}} e^{\frac{V_{\text{D}}}{V_{\text{T}}}}.$$

Putting these two formulae together and considering that the output voltage is the negative of the voltage across the diode ($V_{\text{out}} = -V_{\text{D}}$), the relationship is proven.

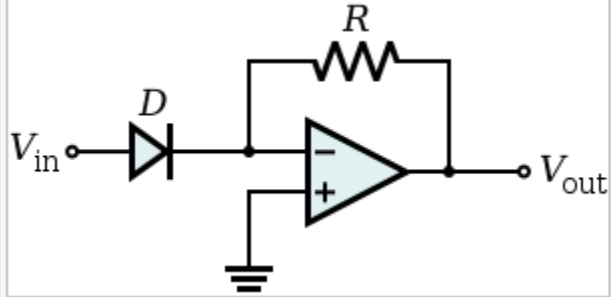
Note that this implementation does not consider temperature stability and other non-ideal effects.

Exponential output

- The relationship between the input voltage v_{in} and the output voltage v_{out} is given by:

$$v_{\text{out}} = -RI_{\text{S}} e^{\frac{v_{\text{in}}}{V_{\text{T}}}}$$

where I_{S} is the *saturation current* and V_{T} is the *thermal voltage*.



Exponential configuration

- Considering the operational amplifier ideal, then the negative pin is virtually grounded, so the current through the diode is given by:

$$I_{\text{D}} = I_{\text{S}} \left(e^{\frac{V_{\text{D}}}{V_{\text{T}}}} - 1 \right)$$

when the voltage is greater than zero, it can be approximated by:

$$I_{\text{D}} \simeq I_{\text{S}} e^{\frac{V_{\text{D}}}{V_{\text{T}}}}.$$

The output voltage is given by:

$$v_{\text{out}} = -RI_{\text{D}}.$$

Other applications

- audio and video pre-amplifiers and buffers
- voltage comparators
- differential amplifiers
- differentiators and integrators
- filters
- precision rectifiers
- voltage regulator and current regulator
- analog-to-digital converter
- digital-to-analog converter
- voltage clamps
- oscillators and waveform generators
- Schmitt trigger
- Gyrator
- Comparator
- Active filter
- Analog computer
- Capacitance multiplier

See also

- Operational amplifier
- Current-feedback operational amplifier
- Operational transconductance amplifier
- Frequency compensation
- George A. Philbrick

References

1. ^ Paul Horowitz and Winfield Hill, *The Art of Electronics*. 2nd ed. Cambridge University Press, Cambridge, 1989 ISBN 0-521-37095-7
2. ^ Basic Electronics Theory, Delton T. Horn, 4th ed. McGraw-Hill Professional, 1994, p.342-343.
3. ^ Malmstadt, Enke and Crouch, Electronics and Instrumentation for Scientists, The Benjamin/Cummings Publishing Company, Inc., 1981, ISBN 0-8053-6917-1, Chapter 5. pp 118.
4. ^ Basic Electronics Theory, Delton T. Horn, 4th ed. McGraw-Hill Professional, 1994, p.342-343.

Further reading

- Paul Horowitz and Winfield Hill, *The Art of Electronics*. 2nd ed. Cambridge University Press, Cambridge, 1989 ISBN 0-521-37095-7
- Sergio Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, 3rd ed., McGraw-Hill, New York, 2002 ISBN 0-07-232084-2

External links

- Introduction to op-amp circuit stages, second order filters, single op-amp bandpass filters, and a simple intercom (http://ourworld.compuserve.com/homepages/Bill_Bowden/opamp.htm)
- Op Amps for Everyone (http://focus.ti.com/lit/an/slod006b/slod006b.pdf) PDF (1.96 MiB)
- Single supply op-amp circuit collection (http://instruct1.cit.cornell.edu/courses/bionb440/datasheets/SingleSupply.pdf) PDF (163 KiB)
- Op-amp circuit collection (http://www.national.com/an/AN/AN-31.pdf) PDF (962 KiB)
- A Collection of Amp Applications (http://www.analog.com/static/imported-files/application_notes/28080533AN106.pdf) PDF (1.06 MiB) – Analog Devices Application note

- Basic OpAmp Applications (http://www.ligo.caltech.edu/~vsanni/ph5/BasicOpAmpApplications.pdf) PDF (173 KiB)
- Handbook of operational amplifier applications (http://focus.ti.com/lit/an/sboa092a/sboa092a.pdf) PDF (2.00 MiB) – Texas Instruments Application note
- Low Side Current Sensing Using Operational Amplifiers (http://focus.ti.com/analog/docs/gencontent.tsp?familyId=57&genContentId=28017)
- Log/anti-log generators, cube generator, multiply/divide amp (http://www.national.com/an/AN/AN-30.pdf) PDF (165 KiB)
- Logarithmically variable gain from a linear variable component (http://www.edn.com/archives/1994/030394/05di7.htm)
- Impedance and admittance transformations using operational amplifiers (http://www.philbrickarchive.org/1964-1_v12_no1_the_lightning_empiricist.htm) by D. H. Sheingold

Retrieved from "http://en.wikipedia.org/wiki/Operational_amplifier_applications"
Categories: Electronic amplifiers | Integrated circuits

Logic gate

From Wikipedia, the free encyclopedia

A **logic gate** performs a logical operation on one or more logic inputs and produces a single logic output. The logic normally performed is Boolean logic and is most commonly found in digital circuits. Logic gates are primarily implemented electronically using diodes or transistors, but can also be constructed using electromagnetic relays, fluidics, optics, molecules, or even mechanical elements.

In electronic logic, a logic level is represented by a voltage or current, (which depends on the type of electronic logic in use). Each logic gate requires power so that it can source and sink currents to achieve the correct output voltage. In logic circuit diagrams the power is not shown, but in a full electronic schematic, power connections are required.

Contents

Truth table

Main article: Truth table

A truth table is a table that describes the behaviour of a logic gate. It lists the value of the output for every possible combination of the inputs and can be used to simplify the number of logic gates and level of nesting in an electronic circuit. In general the truth table does not lead to an efficient implementation; a minimization procedure, using Karnaugh maps, the Quine–McCluskey algorithm or an heuristic algorithm is required for reducing the circuit complexity.

Background

Main article: Logic family

The simplest form of electronic logic is diode logic. This allows AND and OR gates to be built, but not inverters, and so is an incomplete form of logic. Further, without some kind of amplification it is not possible to have such basic logic operations cascaded as required for more complex logic functions. To build a functionally complete logic system, relays, valves (vacuum tubes), or transistors can be used. The simplest family of logic gates using bipolar transistors is called resistor-transistor logic (RTL). Unlike diode logic gates, RTL gates can be cascaded indefinitely to produce more complex logic functions. These gates were used in early integrated circuits. For higher speed, the resistors used in RTL were replaced by diodes, leading to diode-transistor logic (DTL). It was then discovered that one transistor could do the job of two diodes in the space of one diode even better, by more quickly switching off the following stage, so transistor-transistor logic, or TTL, was created. In virtually every type of contemporary chip implementation of digital systems, the bipolar transistors have been replaced by complementary field-effect transistors (MOSFETs) to reduce size and power consumption still further, thereby resulting in complementary metal–oxide–semiconductor (CMOS) logic.

For small-scale logic, designers now use prefabricated logic gates from families of devices such as the TTL 7400 series by Texas Instruments and the CMOS 4000 series by RCA, and their more recent descendants. Increasingly, these fixed-function logic gates are being replaced by programmable logic devices, which allow designers to pack a large number of mixed logic gates into a single integrated circuit. The field-programmable nature of programmable logic devices such as FPGAs has removed the 'hard' property of hardware; it is now possible to change the logic design of a hardware system by reprogramming some of its components, thus allowing the features or function of a hardware implementation of a logic system to be changed.

Electronic logic gates differ significantly from their relay-and-switch equivalents. They are much faster, consume much less power, and are much smaller (all by a factor of a million or more in most cases). Also, there is a fundamental structural difference. The switch circuit creates a continuous metallic path for current to flow (in either direction) between its input and its output. The semiconductor logic gate, on the other hand, acts as a high-gain voltage amplifier, which sinks a tiny current at its input and produces a low-impedance voltage at its output. It is not possible for current to flow between the output and the input of a semiconductor logic gate.

Another important advantage of standardised integrated circuit logic families, such as the 7400 and 4000 families, is that they can be cascaded. This means that the output of one gate can be wired to the inputs of one or several other gates, and so on. Systems with varying degrees of complexity can be built without great concern of the designer for the internal workings of the gates, provided the limitations of each integrated circuit are considered.

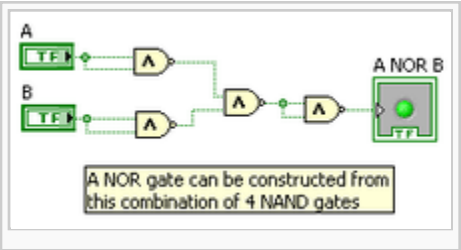
The output of one gate can only drive a finite number of inputs to other gates, a number called the 'fanout limit'. Also, there is always a delay, called the 'propagation delay', from a change in input of a gate to the corresponding change in its output. When gates are cascaded, the total propagation delay is approximately the sum of the individual delays, an effect which can become a problem in high-speed circuits. Additional delay can be caused when a large number of inputs are connected to an output, due to the distributed capacitance of all the inputs and wiring and the finite amount of current that each output can provide.

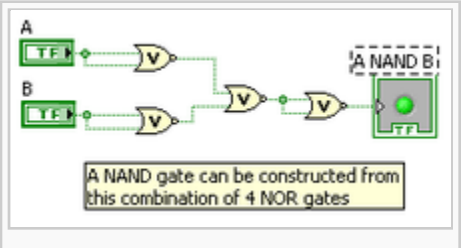
Logic gates

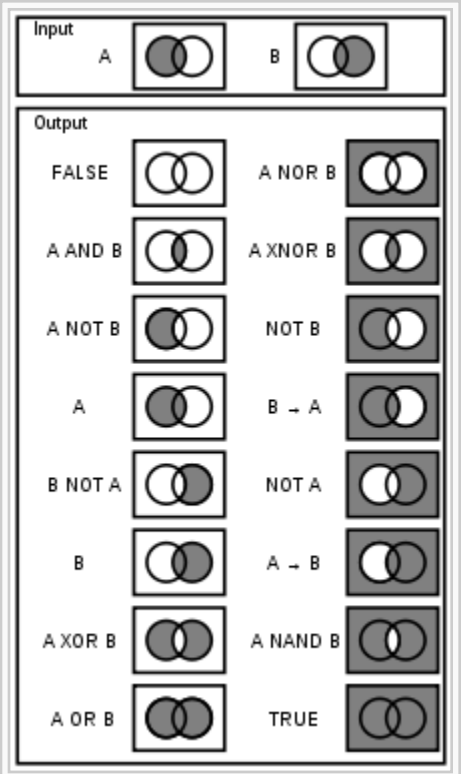
All other types of Boolean logic gates (i.e., AND, OR, NOT, XOR, XNOR) can be created from a suitable network of NAND gates. Similarly all gates can be created from a network of NOR gates. Historically, NAND gates were easier to construct from MOS technology and thus NAND gates served as the first pillar of Boolean logic in electronic computation.

For an input of 2 variables, there are 16 possible boolean algebraic functions. These 16 functions are enumerated below, together with their outputs for each combination of inputs variables.

INPUT	**A**	**0**	**0**	**1**	**1**	**Meaning**
	B	**0**	**1**	**0**	**1**	
OUTPUT	FALSE	0	0	0	0	Whatever *A* and *B*, the output is false. Contradiction.
	A AND B	0	0	0	1	Output is true if and only if (iff) both *A* and *B* are true.
	A $\not\rightarrow$ B	0	0	1	0	*A* doesn't imply *B*. True iff *A* but not *B*.
	A	0	0	1	1	True whenever *A* is true.
	A $\not\leftarrow$ B	0	1	0	0	*A* is not implied by *B*. True iff not *A* but *B*.
	B	0	1	0	1	True whenever *B* is true.
	A XOR B	0	1	1	0	True iff *A* is not equal to *B*.
	A OR B	0	1	1	1	True iff *A* is true, or *B* is true, or both.
	A NOR B	1	0	0	0	True iff neither *A* nor *B*.
	A XNOR B	1	0	0	1	True iff *A* is equal to *B*.
	NOT B	1	0	1	0	True iff *B* is false.
	A $\leftarrow$ B	1	0	1	1	*A* is implied by *B*. False if not *A* but *B*, otherwise true.
	NOT A	1	1	0	0	True iff *A* is false.
	A $\rightarrow$ B	1	1	0	1	*A* implies *B*. False if *A* but not *B*, otherwise true.







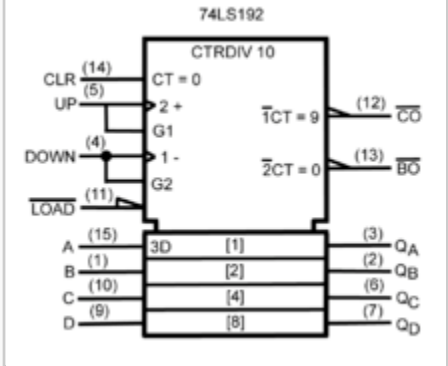
Venn Diagrams for Logic Gates

	A NAND B	1	1	1	0	*A* and *B* are not both true.	
	TRUE	1	1	1	1	Whatever *A* and *B*, the output is true. Tautology.	

The four functions denoted by arrows are the logical implication functions. These functions are generally less common, and are usually not implemented directly as logic gates, but rather built out of gates like AND and OR.

Symbols

There are two sets of symbols in common use, both now defined by ANSI/IEEE Std 91-1984 and its supplement ANSI/IEEE Std 91a-1991. The "distinctive shape" set, based on traditional schematics, is used for simple drawings and is quicker to draw by hand. It is sometimes unofficially described as "military", reflecting its origin if not its modern usage. The "rectangular shape" set, based on IEC 60617-12, has rectangular outlines for all types of gate, and allows representation of a much wider range of devices than is possible with the traditional symbols. The IEC's system has been adopted by other standards, such as EN 60617-12:1999 in Europe and BS EN 60617-12:1999 in the United Kingdom.

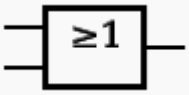
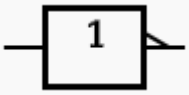
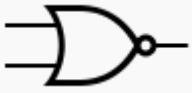
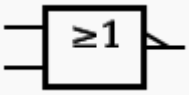


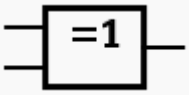
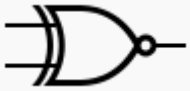
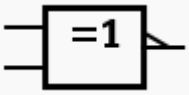
A synchronous 4-bit up/down decade counter symbol (74LS192) in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 60617-12.

The goal of IEEE Std 91-1984 was to provide a uniform method of describing the complex logic functions of digital circuits with schematic symbols. These functions were more complex than simple AND and OR gates. They could be medium scale circuits such as a 4-bit counter to a large scale circuits such as a microprocessor. The 1984 version did not include the "distinctive shape" symbols.[1] (http://focus.ti.com/lit/ml/sdyz001a/sdyz001a.pdf) These were added to the 1991 supplement with this note: "The distinctive-shape symbol is, according to IEC Publication 617, Part 12, not preferred, but is not considered to be in contradiction to that standard."

In the 1980s, schematics were the predominant method to design both circuit boards and custom ICs known as gate arrays. Today custom ICs and the field-programmable gate array are typically designed with Hardware Description Languages (HDL) such as Verilog or VHDL. The need for complex logic symbols has diminished and distinctive shape symbols are still the predominant style.[*citation needed*]

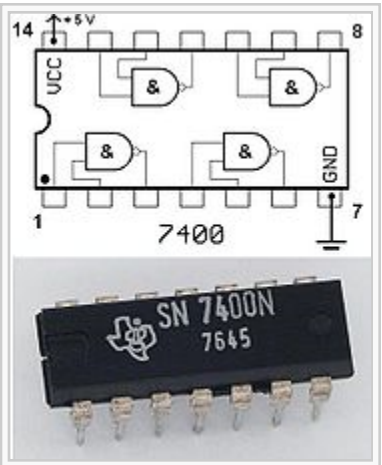
Type	Distinctive shape	Rectangular shape	Boolean algebra between A & B	Truth table
AND			$A \cdot B$	**INPUT** **INPUT** **OUTPUT** A B A AND B

				<table><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>
OR			$A + B$	<table><tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr><tr><td>A</td><td>B</td><td>A OR B</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>
NOT			$\overline{A}$	<table><tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr><tr><td colspan="2">A</td><td>NOT A</td></tr><tr><td colspan="2">0</td><td>1</td></tr><tr><td colspan="2">1</td><td>0</td></tr></table>
In electronics a NOT gate is more commonly called an inverter. The circle on the symbol is called a *bubble*, and is generally used in circuit diagrams to indicate an inverted (active-low) input or output.[1]				
NAND			$\overline{A \cdot B}$	<table><tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr><tr><td>A</td><td>B</td><td>A NAND B</td></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>
NOR			$\overline{A + B}$	<table><tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr><tr><td>A</td><td>B</td><td>A NOR B</td></tr><tr><td>0</td><td>0</td><td>1</td></tr></table>

				0 1 0 1 0 0 1 1 0
XOR			$A \oplus B$	INPUT OUTPUT A B A XOR B 0 0 0 0 1 1 1 0 1 1 1 0
XNOR			$\overline{A \oplus B}$	INPUT OUTPUT A B A XNOR B 0 0 1 0 1 0 1 0 0 1 1 1

In practice, the cheapest gate to manufacture is usually the NAND gate. Additionally, Charles Sanders Peirce (1880) showed that NAND gates alone (as well as NOR gates alone) can be used to reproduce the functions of all the other logic gates, but his work on it was unpublished until 1935. The first published proof was by Henry M. Sheffer in 1913.

Two more gates are the exclusive-OR or XOR function and its inverse, exclusive-NOR or XNOR. The two input Exclusive-OR is true only when the two input values are *different*, false if they are equal, regardless of the value. If there are more than two inputs, the gate generates a true at its output if the number of trues at its input is *odd* ([2] (http://www-inst.eecs.berkeley.edu/~cs61c/resources/dg-BOOL-handout.pdf)). In practice, these gates are built from combinations of simpler logic gates.



The 7400 chip, containing four NANDs. The two additional pins supply power (+5 V) and connect the ground.

De Morgan equivalent symbols

By use of De Morgan's theorem, an *AND* gate can be turned into an *OR* gate by inverting the sense of the logic at its inputs and outputs. This leads to a separate set of symbols with inverted inputs and the opposite core symbol. These symbols can make circuit diagrams for circuits using active low signals much clearer and help to show accidental connection of an active high output to an active low input or vice-versa.

Symbolically, a NAND gate can also be shown using the OR shape with bubbles on its inputs, and a NOR gate can be shown as an AND gate with bubbles on its inputs. The bubble signifies a logic inversion. This reflects the equivalency due to De Morgans law, but it also allows a diagram to be read more easily, or a circuit to be mapped onto available physical gates in packages easily, since any circuit node that has bubbles at both ends can be replaced by a simple bubble-less connection and a suitable change of gate. If the NAND is drawn as OR with input bubbles, and a NOR as AND with input bubbles, this gate substitution occurs automatically in the diagram (effectively, bubbles "cancel"). This is commonly seen in real logic diagrams - thus the reader must not get into the habit of associating the shapes exclusively as OR or AND shapes, but also take into account the bubbles at both inputs and outputs in order to determine the "true" logic function indicated.

All logic relations can be realized by using NAND gates (this can also be done using NOR gates). De Morgan's theorem is most commonly used to transform all logic gates to NAND gates or NOR gates. This is done mainly since it is easy to buy logic gates in bulk and because many electronics labs stock only NAND and NOR gates.

Storage of bits

Main article: sequential logic

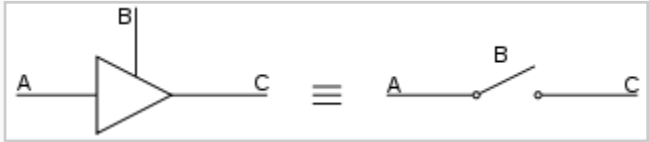
Related to the concept of logic gates (and also built from them) is the idea of storing a bit of information. None of the gates discussed up to here can store a value by itself: when the inputs change, the outputs immediately react. It is possible to make a storage element either through a capacitor (which stores charge due to its physical properties) or by feedback. Connecting the output of a gate to the input causes it to be put through the logic again, and choosing the feedback correctly allows it to be preserved or modified through the use of other inputs. A set of gates arranged in this fashion is known as a "latch", and more complicated designs that utilize clock signals and change only on the rising edge are called edge-triggered "flip-flops". The combination of multiple flip-flops in parallel, to store a multiple-bit value, is known as a register. When using any of these gate setups the overall system has memory; it is then called a sequential logic system since its output can be influenced by its previous state(s).

These registers or capacitor-based circuits are known as computer memory. They vary in performance, based on factors of speed, complexity, and reliability of storage, and many different types of designs are used based on

the application.

Three-state logic gates

Main article: Tri-state buffer



A tristate buffer can be thought of as a switch. If *B* is on, the switch is closed. If B is off, the switch is open.

Three-state, or 3-state, logic gates are a type of logic gates that have three states of the output: high (H), low (L) and high-impedance (Z). The high-impedance state plays no role in the logic, which remains strictly binary. These devices are used on buses also known as the Data Buses of the CPU to allow multiple chips to send data. A group of three-states driving a line with a suitable control circuit is basically equivalent to a multiplexer, which may be physically distributed over separate devices or plug-in cards.

In electronics, a high output would mean the output is sourcing current from the positive power terminal (positive voltage). A low output would mean the output is sinking current to the negative power terminal (zero voltage). High impedance would mean that the output is effectively disconnected from the circuit.

'Tri-state', a widely-used synonym of 'three-state', is a trademark of the National Semiconductor Corporation.

Miscellaneous

Logic circuits include such devices as multiplexers, registers, arithmetic logic units (ALUs), and computer memory, all the way up through complete microprocessors, which may contain more than 100 million gates. In practice, the gates are made from field-effect transistors (FETs), particularly MOSFETs.

Compound logic gates AND-OR-Invert (AOI) and OR-AND-Invert (OAI) are often employed in circuit design because their construction using MOSFET's is simpler and more efficient than the sum of the individual gates.[2]

In reversible logic, Toffoli gates are used.

History and development

The earliest logic gates were made mechanically. Charles Babbage, around 1837, devised the Analytical Engine. His logic gates relied on mechanical gearing to perform operations. Electromagnetic relays were later used for logic gates. In 1891, Almon Strowger patented a device containing a logic gate switch circuit (U.S. Patent 0,447,918 (http://www.google.com/patents?vid=447918)). Strowger's patent was not in widespread use until the 1920s. Starting in 1898, Nikola Tesla filed for patents of devices containing logic gate circuits (see List of Tesla patents). Eventually, vacuum tubes replaced relays for logic operations. Lee De Forest's modification, in 1907, of the Fleming valve can be used as AND logic gate. Ludwig Wittgenstein introduced a version of the 16-row truth table, which is shown above, as proposition 5.101 of *Tractatus Logico-Philosophicus* (1921). Claude E. Shannon introduced the use of Boolean algebra in the analysis and design of switching circuits in 1937. Walther Bothe, inventor of the coincidence circuit, got part of the 1954 Nobel Prize in physics, for the first modern electronic AND gate in 1924. Active research is taking place in molecular logic gates.

Implementations

As of 2008, most logic gates are made of CMOS transistors. Often millions of logic gates are packaged in a single integrated circuit.

There are several logic families with different characteristics (power consumption, speed, cost, size) such as: RDL (resistor-diode logic), RTL (resistor-transistor logic), DTL (diode-transistor logic), TTL (transistor-transistor logic) and CMOS (complementary metal oxide semiconductor).

Many early electromechanical digital computers, such as the Harvard Mark I, were built from relay logic gates, using electro-mechanical relays.

It is also possible to make logic gates out of pneumatic devices, such as the Sorteberg relayor mechanical logic gates, including on a molecular scale.[3] Logic gates have been made out of DNA (see DNA nanotechnology)[4] and used to create a computer called MAYA (see MAYA II).

Additionally, logic gates can be made from quantum mechanical effects (though quantum computing usually diverges from boolean design).

It is also possible to make photonic logic gates using non-linear optical effects.[*citation needed*]

See also

- And-inverter graph
- Boolean algebra topics
- Boolean function
- Digital circuit
- Espresso heuristic logic minimizer
- Fanout
- Flip-flop (electronics)
- Karnaugh map
- Logic family
- Logical graph
- NMOS logic
- Propositional calculus
- Race hazard
- Reversible computing
- Truth table

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2. ^ Tinder, Richard F. (2000). *Engineering digital design: Revised Second Edition* (http://books.google.com/books?id=6x0pjjMKRh0C&pg=PT347&lpg=PT347&dq=AOI+gate&source=web&ots=t-wt6hoi1-&sig=dlnF_Kq9jYe27dbr7Rb5gThgM2Y&hl=en&sa=X&oi=book_result&resnum=7&ct=result#PPT346,M1) . pp. 317–319. ISBN 0126912955. http://books.google.com/books?id=6x0pjjMKRh0C&pg=PT347&

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3. ^ Mechanical Logic gates (focused on molecular scale) (http://www.zyvex.com/nanotech/mechano.html)
4. ^ DNA Logic gates (https://digamma.cs.unm.edu/wiki/bin/view/McogPublicWeb/MolecularLogicGates)

- *Symbols for logic gates (http://www.uq.edu.au/_School_Science_Lessons/39.4.01.GIF)* . Twenty First Century Books, Breckenridge, CO.
- *Wireless Remote Control and the Electronic Computer Logic logic elements (http://www.tfcbooks.com /articles/control.htm)*

Further reading

- Awschalom, D., D. Loss, and N. Samarth, *Semiconductor Spintronics and Quantum Computation* (2002), Springer-Verlag, Berlin, Germany.
- Bostock, Geoff, *Programmable Logic Devices. Technology and Applications* (1988), McGraw-Hill, New York, NY.
- Brown, Stephen D. et al., *Field-Programmable Gate Arrays* (1992), Kluwer Academic Publishers, Boston, MA.

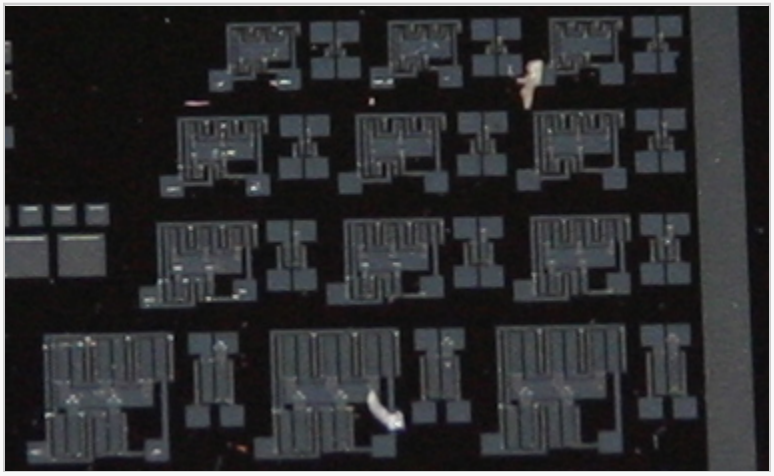
External links

- Online logic gate simulator (http://www.neuroproductions.be/logic-lab/index.php?id=52)
- Java applet of NOT gate (http://www.phy.hk/wiki/englishhtm/NotGate.htm)
- LogicCircuit – is free educational software for designing and simulating digital logic circuits. (http://www.logiccircuit.org/)
- Logic Gate Simulator in Adobe Flex (http://joshblog.net/projects/logic-gate-simulator/Logicly.html)

Ring oscillator

From Wikipedia, the free encyclopedia

A **ring oscillator** is a device composed of an odd number of NOT gates whose output oscillates between two voltage levels, representing *true* and *false*. The NOT gates, or inverters, are attached in a chain; the output of the last inverter is fed back into the first.



Ring oscillators fabricated on silicon using p-type MOSFETs.

Applications

The voltage-controlled oscillator in most phase locked loops is built from a ring oscillator.[1]

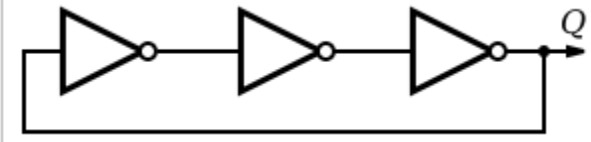
A ring oscillator is often used to demonstrate a new hardware technology, analogous to the way a hello world program is often used to demonstrate a new software technology.[2][3]

Many wafers include a ring oscillator as part of the scribe line test structures. They are used during wafer testing to measure the effects of manufacturing process variations.[4]

Ring oscillators can also be used to measure the effects of voltage and temperature on a chip.[5]

Details

Because a single inverter computes the logical NOT of its input, it can be shown that the last output of a chain of an odd number of inverters is the logical NOT of the first input. This final output is asserted a finite amount of time after the first input is asserted; the feedback of this last output to the input causes oscillation.



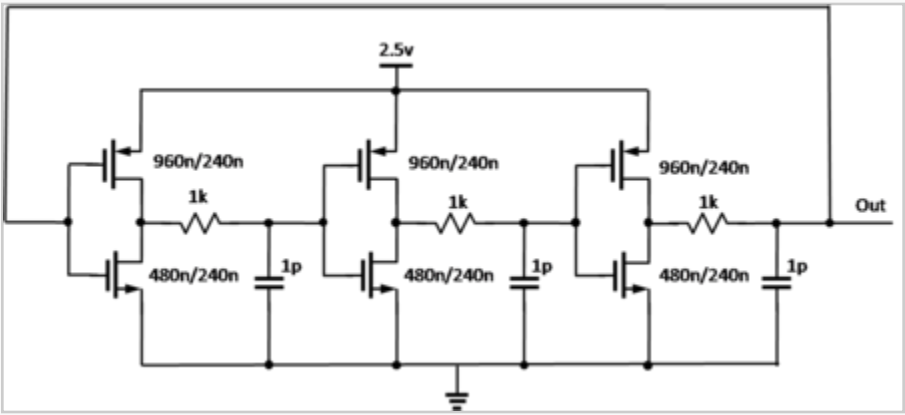
A schematic of a simple 3-inverter ring oscillator whose output frequency is 1/(6×inverter delay).

A circular chain composed of an even number of inverters cannot be used as a ring oscillator; the last output in this case is the same as the input. However, this configuration of inverter feedback can be used as a storage element; it is the basic building block of static random access memory, or SRAM.

A real ring oscillator only requires power to operate; above a certain threshold voltage, oscillations begin spontaneously. To increase the frequency of oscillation, two methods may be used. Firstly, the applied voltage may be increased; this increases both the frequency of the oscillation and the power consumed, which is dissipated as heat. The heat dissipated limits the speed of a given oscillator. Secondly, a smaller ring oscillator may be fabricated; this results in a higher frequency of oscillation given a certain power consumption.

To understand the operation of a ring oscillator, one must first understand gate delay. In a physical device, no

gate can switch instantaneously; in a device fabricated with MOSFETs, for example, the gate capacitance must be charged before current can flow between the source and the drain. Thus, the output of every inverter of a ring oscillator changes a finite amount of time after the input has changed. From here, it can be easily seen that adding more inverters to the chain increases the total gate delay, reducing the frequency of oscillation.



A transistor level schematic of a three stage ring oscillator with delay in a .25u CMOS process.

The ring oscillator is a member of the class of time delay oscillators. A time delay oscillator consists of an inverting amplifier with a delay element between the amplifier output and its input. The amplifier must have a gain of greater than 1.0 at the intended oscillation frequency. Consider the initial case where the amplifier input and output voltages are momentarily balanced at a stable point. A small amount of noise can cause the amplifier output to rise slightly. After passing through the time delay element, this small output voltage change will be presented to the amplifier input. The amplifier has a negative gain of greater than 1, so the output will change in the direction opposite to this input voltage. It will change by an amount larger than the input value, for a gain of greater than 1. This amplified, reversed signal propagates from the output through the time delay and back to the input, where it is amplified and inverted again. The result of this sequential loop is a square wave signal at the amplifier output with the period of each half of the square wave equal to the time delay. The square wave will grow until the amplifier output voltage reaches its limits, where it will stabilize. A more exact analysis will show that the wave that grows from the initial noise may not be square as it grows, but it will become square as the amplifier reaches its output limits.

The ring oscillator is a distributed version of the delay oscillator. The ring oscillator uses an odd number of inverters to give the effect of a single inverting amplifier with a gain of greater than one. Rather than having a single delay element, each inverter contributes to the delay of the signal around the ring of inverters, hence the name ring oscillator. Adding pairs of inverters to the ring increases the total delay and thereby decreases the oscillator frequency. Changing the supply voltage changes the delay through each inverter, with higher voltages typically decreasing the delay and increasing the oscillator frequency.

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2. ^ Slashdot Science: "IBM Creates Ring Oscillator on a Single Nanotube" (http://science.slashdot.org/article.pl?sid=06/03/24/015207)
3. ^ Slashdot Hardware: "World's First Completely Transparent IC" (http://hardware.slashdot.org/article.pl?sid=06/03/20/223206)
4. ^ "Ring oscillators for CMOS process tuning and variability control" (http://cat.inist.fr/?aModele=afficheN&cpsidt=17502322) by BHUSHAN Manjul; GATTIKER Anne; KETCHEN Mark B.; DAS Koushik K.
5. ^ "Analysis of a ring oscillator based on-chip thermal sensor" (http://www-unix.ecs.umass.edu/~dkumar/lab4_658_report/lab4_report.htm)

Categories: Digital circuits | Oscillators

Latch (electronics)

From Wikipedia, the free encyclopedia

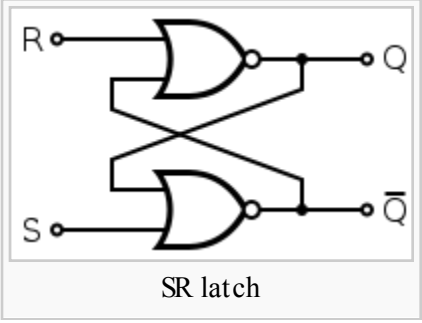
In electronics, a **latch** is a kind of **bistable multivibrator**, an electronic circuit which has two stable states and thereby can store one bit of information. Today the word is mainly used for simple *transparent* storage elements, while slightly more advanced *non-transparent* (or *clocked*) devices are described as **flip-flops**. Informally, as this distinction is quite new, the two words are sometimes used interchangeably.

A circuit incorporating latches has state; its output may depend not only on its current input, but also on its previous inputs. Such a circuit is described as sequential logic.

Contents

Simple set-reset latches

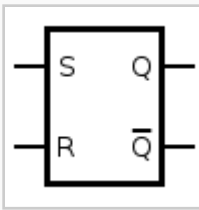
When using static gates as building blocks, the most fundamental latch is the simple *SR latch*, where S and R stand for *set* and *reset*. It can be constructed from a pair of cross-coupled NOR (Not OR) logic gates. The stored bit is present on the output marked Q.



SR latch

Normally, in storage mode, the S and R inputs are both low, and feedback maintains the Q and $\overline{Q}$ outputs in a constant state, with $\overline{Q}$ the complement of Q. If S (*Set*) is pulsed high while R (*Reset*) is held low, then the Q output is forced high, and stays high when S returns to low; similarly, if R is pulsed high while S is held low, then the Q output is forced low, and stays low when R returns to low.

SR latch operation		
S	**R**	**Action**
0	0	Keep state
0	1	Q = 0
1	0	Q = 1
1	1	Restricted combination



The symbol for an SR latch.

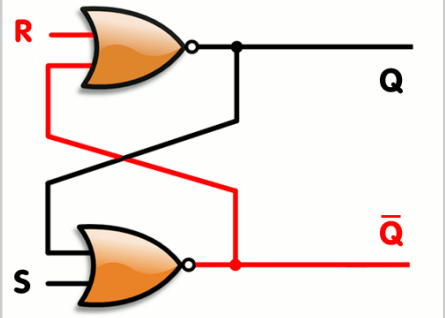


Illustration of SR latch operation. Red and black mean logical '1' and '0', respectively.

The R = S = 1 combination is called a **restricted combination** or a **forbidden state** because, as both NOR gates then output zeros, it breaks the logical equation Q = **not** $\overline{Q}$. The combination is also inappropriate in circuits where *both* inputs may go low *simultaneously* (i.e. a transition from *restricted* to *keep*). The output would lock at either 1 or 0 depending on the propagation time relations between the gates (a race condition). In certain implementations, it could also lead to longer ringings (damped oscillations) before the output settles, and thereby result in undetermined values (errors) in high-frequency digital circuits. This condition is therefore usually avoided.

To overcome the restricted combination, one can add gates to the inputs that would convert `(S,R) = (1,1)` to one of the non-restricted combinations. That can be:

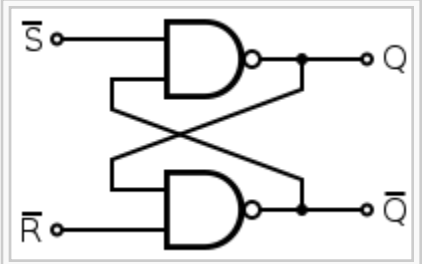
- Q = 1 (1,0) – referred to as an *S-latch*
- Q = 0 (0,1) – referred to as an *R-latch*
- Keep state (0,0) – referred to as an *E-latch*

Alternatively, the restricted combination can be made to *toggle* the output. The result is the JK latch.

Characteristic: Q+ = R'Q + R'S or Q+ = R'Q + S[1]

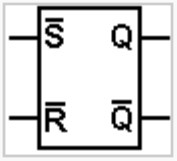
$\overline{SR}$ NAND latch

This is an alternate model of the simple SR latch built with NAND (not AND) logic gates. *Set* and *reset* now become active low signals, denoted $\overline{S}$ and $\overline{R}$ respectively. Otherwise, operation is identical to that of the SR latch. Historically, $\overline{SR}$-latches have been predominant despite the notational inconvenience of active-low inputs. This is because NAND gates are cheaper to produce than NOR gates in the diode-transistor logic (DTL) and transistor-transistor logic (TTL) families, which were the basis of early integrated circuits before the complementary metal–oxide semiconductor (CMOS) family attained widespread use. Since the 1970s and still as of 2009, most integrated circuits are built using CMOS technology, where NAND gates are also preferred.



$\overline{SR}$ latch

$\overline{SR}$ latch operation		
$\overline{S}$	$\overline{R}$	Action
0	0	Restricted combination
0	1	Q = 1
1	0	Q = 0
1	1	Keep state



Symbol for an $\overline{SR}$ NAND latch

JK latch

The JK latch is much less used than the JK Flip-flop. The JK latch follows the following state table:

JK Latch truth table			
J	K	Q_{next}	Comment
0	0	Q_{prev}	No change
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q}_{prev}$	Toggle

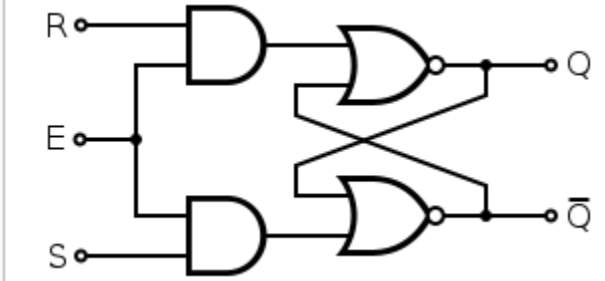
Hence, the JK latch is identical to an SR latch that is made to *toggle* its output when passed the restricted combination.

Gated latches and conditional transparency

Latches are designed to be *transparent*. That is, input signal changes cause immediate changes in output.[nb 1] Alternatively, additional logic can be added to a simple transparent latch to make it *non-transparent* or *opaque* when another input (e.g., an "enable" input) is not asserted. By following a *transparent-high* latch with a *transparent-low* (or *opaque-high*) latch, a simple *edge-triggered* flip-flop can be implemented.[*citation needed*]

Gated SR latch

A *synchronous SR latch* (sometimes *clocked SR flip-flop*) can be made by adding a second level of NAND gates to the inverted SR latch (or a second level of NOR gates to the direct SR latch). The extra gates further invert the inputs so the simple $\overline{SR}$ latch becomes a gated $\overline{SR}$ latch (and a simple SR latch would transform into a gated $\overline{SR}$ latch with inverted enable).



A gated SR latch circuit diagram constructed from NOR gates.

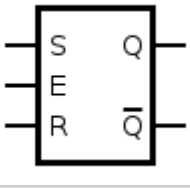
With E high (*enable* true), the signals can pass through the input gates to the encapsulated latch; all signal combinations except for (0,0) = *hold* then immediately reproduce on the (Q,$\overline{Q}$) output, i.e. the latch is *transparent*.

With E low (*enable* false) the latch is *closed (opaque)* and remains in the state it was left the last time E was high.

The *enable* input is sometimes a clock signal, but more often a read or write strobe.

Gated SR latch operation

E/C	Action
0	No action (keep state)
1	The same as non-clocked SR latch

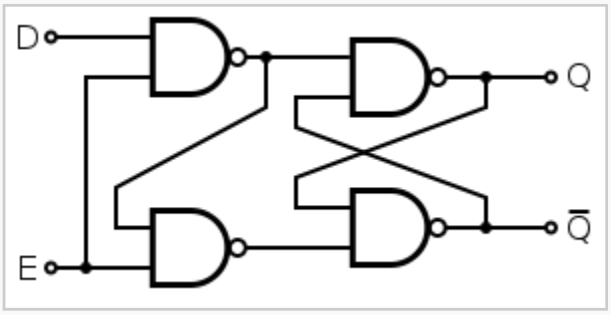


symbol for a gated SR latch

Gated D-latch

This latch is closely related to the gated SR latch and can be similarly constructed. It is also known as *transparent latch*, *data latch*, or simply *gated latch*. It has a *data* input and an *enable* signal (sometimes named *clock*, or *control*). The word *transparent* comes from the fact that, when the enable input is on, the signal propagates directly through the circuit, from the input D to the output Q.

Transparent latches are typically used as I/O ports or in asynchronous systems.[nb 2] They are available as integrated circuits, usually with multiple latches per circuit. For example, 74HC75 is a quadruple transparent latch in the ubiquitous 7400 series.

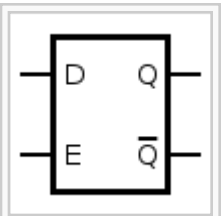


A D-type transparent latch

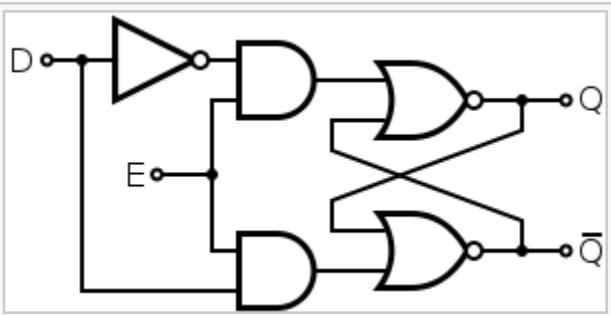
D	Input
E	Enable/clock
Q	Output
$\overline{\mathbf{Q}}$	Inverse of Q

D-latch truth table

E/C	D	Q	$\overline{Q}$	Comment
0	X	Q_{prev}	$\overline{Q}_{prev}$	No change
1	0	0	1	Reset
1	1	1	0	Set



Symbol for a gated D latch



A gated D latch based on SR (NOR) latch

The truth table shows that when the *e*nable/*c*lock input is 0, the D input has no effect on the output. When E/C is high, the output equals D.

Gated T-Latch

This is another synchronous SR latch that toggles the previous output. If the toggle (T) input is high, the T latch (well known as T flip-flop) changes state ("toggles") whenever the clock input is strobed. If the T input is low, it holds the previous value. Characteristic equation is; $Q_{next} = T \oplus Q_{pre}$, where Q_{next} is the next state and Q_{prev} is the previous state.

T	Q_{prev}	Q_{next}	Comment
0	0	0	Hold state
0	1	1	
1	0	1	Toggle state
1	1	0	

A T flip-flop can also be built using a JK flip-flop (i.e., with T implemented by connecting J & K pins together) or D flip-flop (T input and $Q_{previous}$ is connected to the D input through an XOR gate).

Notes

1. ^ Note that when several *transparent* latches follow each other, signals propagate through all of them.
2. ^ Transparent latches are also sometimes used in synchronous two-phase systems (for reduced transistor count); however, in single-phase synchronous systems with direct feedback, master-slave devices (often edge-triggered) must be used to avoid analog oscillations.

References

1. ^ http://books.google.com/books?id=4sX9fTGRo7QC&pg=PA344&lpg=PA344&dq=sr+characteristic+latch+equation&source=web&ots=9WdHN5uzTF&sig=ewGWuNX8g_4KozJuL5VyAS2yErc#PPA343,M1

See also

- Flip-flop
- Logic gate

Further reading

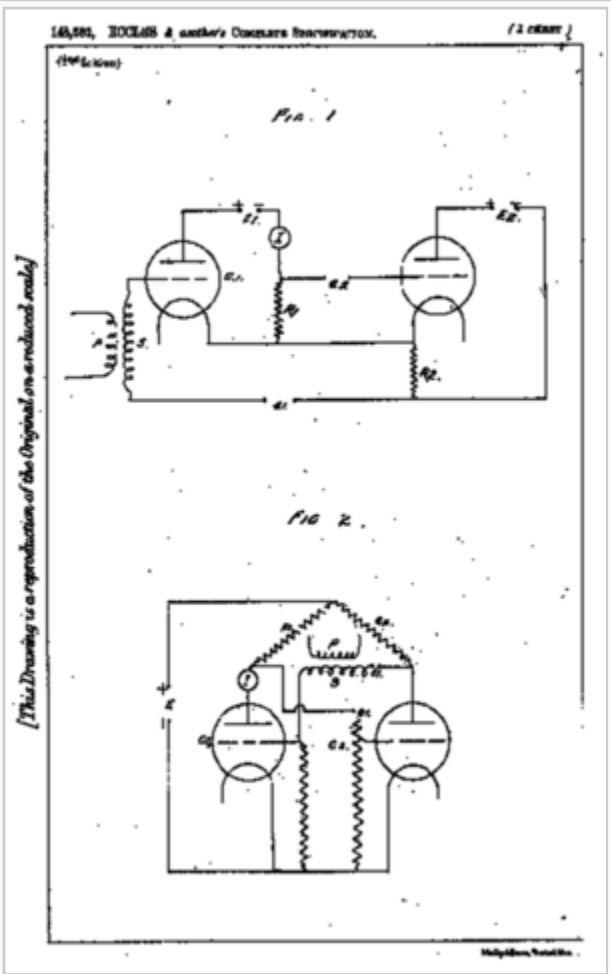
- Hwang, Enoch (2006). *Digital Logic and Microprocessor Design with VHDL* (http://faculty.lasierra.edu/~ehwang/digitaldesign) . Thomson. ISBN 0-534-46593-5. http://faculty.lasierra.edu/~ehwang/digitaldesign.
- Fundamentals of Digital Logic by Brown and Vranesic
- S.P.Vingron: "Switching Theory. Insight through Predicate Logic". Springer Verlag, 2003. ISBN 3-540-40343-4 – extensively covers the theory of latches
- Parallel Port Output expanding with Latches (http://www.globu.net/pp/english/pp/)
- CircuitDesign.info: You want latches? We got latches (http://www.circuitdesign.info/blog/2008/12/you-want-latches-we-got-latches-flip-flop-design/) CMOS D flip-flop design
- V. O. Vasyukevich. "Analytics of trigger functions". *Automatic Control and Computer Sciences* (http://www.springerlink.com/content/3h040562h73855w5/) . 2009, Vol.43, No.4, 184–189.

Flip-flop (electronics)

From Wikipedia, the free encyclopedia

In digital circuits, a **flip-flop** is a term referring to an electronic circuit (a bistable multivibrator) that has two stable states and thereby is capable of serving as one bit of memory. Today, the term *flip-flop* has come to mostly denote *non-transparent* (*clocked* or *edge-triggered*) devices, while the simpler *transparent* ones are often referred to as latches; however, as this distinction is quite new, the two words are sometimes used interchangeably (see history).

A flip-flop is usually controlled by one or two control signals and/or a gate or clock signal. The output often includes the complement as well as the normal output. As flip-flops are implemented electronically, they require power and ground connections.



Flip-flop schematics from the Eccles and Jordan patent filed 1918, one drawn as a cascade of amplifiers with a positive feedback path, and the other as a symmetric cross-coupled pair

Contents

History

The first electronic flip-flop was invented in 1918 by William Eccles and F. W. Jordan.[1][2] It was initially called the *Eccles–Jordan trigger circuit* and consisted of two active elements (electron tubes). The name

flip-flop was later derived from the sound produced on a speaker connected to one of the back-coupled amplifiers outputs during the trigger process within the circuit.[*citation needed*] This original *electronic* flip-flop—a simple two-input bistable circuit without any dedicated clock (or even gate) signal, was *transparent*, and thus a device that would be labeled as a "latch" in many circles today.

The flip-flop types discussed below (D, RS, JK, T) were first discussed in a 1954 UCLA course on computer design by Montgomery Phister,[*citation needed*] and in his book *Logical Design of Digital Computers*.[3] The author was at the time working at Hughes Aircraft under Dr. Eldred Nelson, who had coined the term JK for a flip-flop which changed states when both inputs were on.[*citation needed*] The other names were coined by Phister. They differ slightly from some of the definitions given below.

The origin of the name for the JK flip-flop is detailed by P. L. Lindley, a JPL engineer, in a letter to *EDN*, an electronics design magazine. The letter is dated June 13, 1968, and was published in the August edition of the newsletter. In the letter, Mr. Lindley explains that he heard the story of the JK flip-flop from Dr. Eldred Nelson, who is responsible for coining the term while working at Hughes Aircraft. Flip-flops in use at Hughes at the time were all of the type that came to be known as J-K. In designing a logical system, Dr. Nelson assigned letters to flip-flop inputs as follows: #1: A & B, #2: C & D, #3: E & F, #4: G & H, #5: J & K.

Implementation

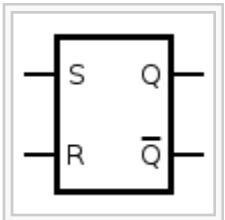
Flip-flops can be either simple (transparent) or clocked. Simple flip-flops can be built around a pair of cross-coupled *inverting* elements: vacuum tubes, bipolar transistors, field effect transistors, inverters, and inverting logic gates have all been used in practical circuits—perhaps augmented by some gating mechanism (an enable/disable input). The more advanced clocked (or non-transparent) devices are specially designed for synchronous (time-discrete) systems; such devices therefore ignore its inputs except **at** the transition of a dedicated clock signal (known as clocking, pulsing, or strobing). This causes the flip-flop to either change or retain its output signal based upon the values of the input signals at the transition. Some flip-flops change output on the rising edge of the clock, others on the falling edge.

Clocked flip-flops are typically implemented as master–slave devices[4] where two basic flip-flops (plus some additional logic) collaborate to make it insensitive to spikes and noise between the short clock transitions; they nevertheless also often include asynchronous *clear* or *set* inputs which may be used to change the current output independent of the clock.

Flip-flops can be further divided into types that have found common applicability in both asynchronous and clocked sequential systems: the **SR** ("set-reset"), **D** ("data" or "delay"[5]), **T** ("toggle"), and **JK** types are the common ones; all of which may be synthesized from (most) other types by a few logic gates. The behavior of a particular type can be described by what is termed the characteristic equation, which derives the "next" (i.e., after the next clock pulse) output, Q_{next}, in terms of the input signal(s) and/or the current output, Q.

SR flip-flops

The fundamental latch is the simple *SR flip-flop* (also commonly known as *RS flip-flop*), where S and R stand for *set* and *reset*, respectively. It can be constructed from a pair of cross-coupled NAND or NOR logic gates. The stored bit is present on the output marked Q.



The symbol for an SR latch

Normally, in storage mode, the S and R inputs are both low, and feedback maintains the Q and $\overline{Q}$ outputs in a constant state, with $\overline{Q}$ the complement of Q. If S is pulsed high while R is held low, then the Q output is forced high, and stays high even after S returns low; similarly, if R is pulsed high while S is held low, then the Q output is forced low, and stays low even after R returns low.

The next-state equation of the SR flip-flop is

$$Q_{next} = S + \overline{R}Q$$

where Q is the current state .Q_{next} becomes Q (the stored value) at clock edge.

SR Flip-Flop operation (BUILT WITH NOR GATES) [6]							
Characteristic table			**Excitation table**				
S	**R**	**Action**	**Q(t)**	**Q(t+1)**	**S**	**R**	**Action**
0	0	Keep state	0	0	0	X	No change
0	1	Q = 0	1	0	0	1	reset
1	0	Q = 1	0	1	1	0	set
1	1	Race Condition	1	1	X	0	No Change

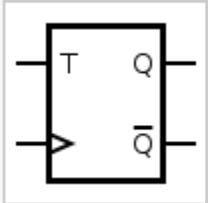
('X' denotes a Don't care condition; meaning the signal is irrelevant)

T flip-flops

If the T input is high, the T flip-flop changes state ("toggles") whenever the clock input is strobed. If the T input is low, the flip-flop holds the previous value. This behavior is described by the characteristic equation:

$$Q_{next} = T \oplus Q = T\overline{Q} + \overline{T}Q \text{ expanding the XOR operator}$$

and can be described in a truth table:

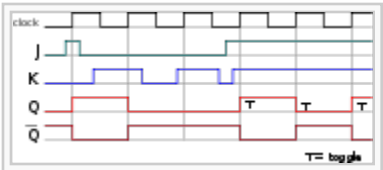


A circuit symbol for a T-type flip-flop, where > is the clock input, T is the toggle input and Q is the stored data output

T Flip-Flop operation [6]							
Characteristic table				**Excitation table**			
T	***Q***	***Q*next***	**Comment**	***Q***	***Q*next***	***T***	**Comment**
0	0	0	hold state (no clk)	0	0	0	No change
0	1	1	hold state (no clk)	1	1	0	No change
1	0	1	toggle	0	1	1	Complement
1	1	0	toggle	1	0	1	Complement

When T is held high, the toggle flip-flop divides the clock frequency by two; that is, if clock frequency is 4 MHz, the output frequency obtained from the flip-flop will be 2 MHz. This "divide by" feature has application in various types of digital counters. A T flip-flop can also be built using a JK flip-flop (J & K pins are connected together and act as T) or D flip-flop (T input and $Q_{previous}$ is connected to the D input through an XOR gate).

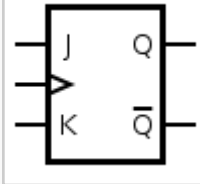
JK flip-flop



JK flip-flop timing diagram

The JK flip-flop augments the behavior of the SR flip-flop (J=Set, K=Reset) by interpreting the S = R = 1 condition as a "flip" or toggle command. Specifically, the combination J = 1, K = 0 is a command to set the flip-flop; the combination J = 0, K = 1 is a command to reset the flip-flop; and the combination J = K = 1 is a command to toggle the flip-flop, i.e., change its output to the logical complement of its current value. Setting J = K = 0 does NOT result in a D flip-flop, but rather, will hold the current state. To synthesize a D flip-flop, simply set K equal to the complement of J. The JK flip-flop is therefore a universal flip-flop, because it can be configured to work as an SR flip-flop, a D flip-flop, or a T flip-flop.

NOTE: The flip-flop is positive-edge triggered (rising clock pulse) as seen in the timing diagram.



A circuit symbol for a **negative edge triggered** JK flip-flop, where > is the clock input, J and K are data inputs, Q is the stored data output, and Q' is the inverse of Q

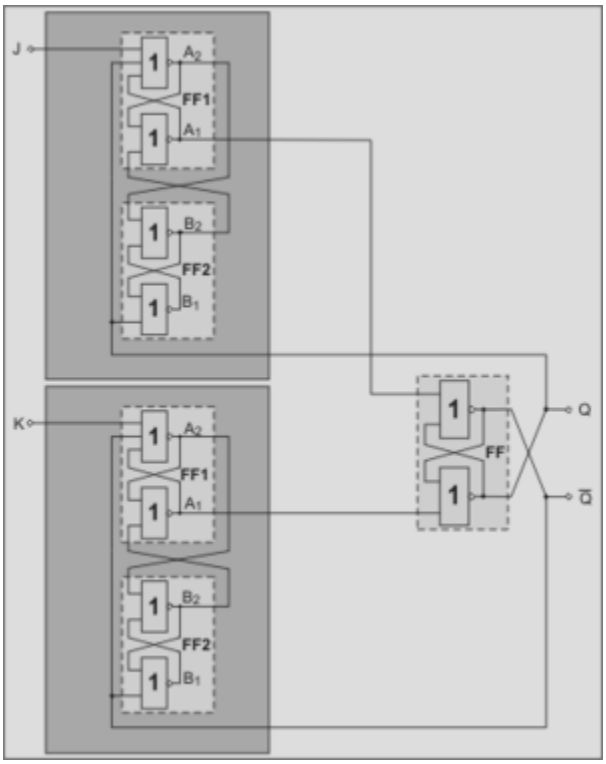
The characteristic equation of the JK flip-flop is:

$$Q_{next} = J\overline{Q} + \overline{K}Q$$

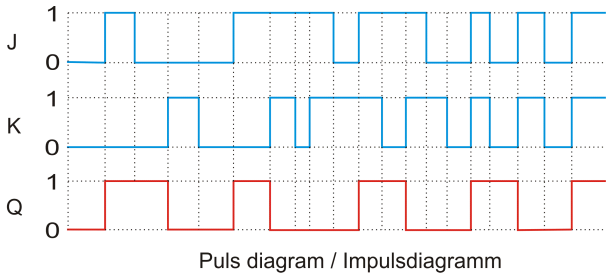
and the corresponding truth table is:

JK Flip Flop operation [6]								
Characteristic table				**Excitation table**				
J	**K**	**Q_{next}**	**Comment**	**Q**	**Q_{next}**	**J**	**K**	**Comment**
0	0	Q_{prev}	hold state	0	0	0	X	No change
0	1	0	reset	0	1	1	X	Set
1	0	1	set	1	0	X	1	Reset
1	1	$\overline{Q}_{prev}$	toggle	1	1	X	0	No change

More to JK flip-flops

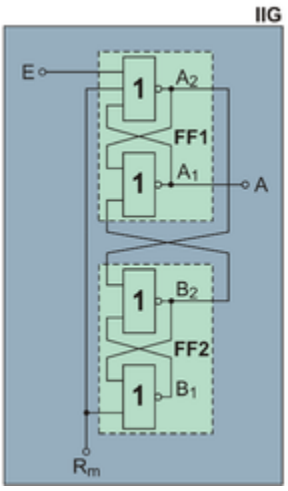


In literature and on the internet it is generally assumed that JK flip-flops need a clock signal. This needs not to be so. A non-clocked JK flip-flop circuit was developed by Klaus-Eckart Schulz in the years 1980/1981. The circuit is pictured on the left, based on NOR gates. This circuit implements the typical characteristics of a JK flip-flop: a change from 0 to 1 at the J input sets the flip-flop (Q = 1), a change from 0 to 1 at the K input resets the flip-flop (Q = 0). If both inputs are combined, with every change of 0 to 1 at the inputs, the flip-flop output Q will be inverted. That is, the flip-flop operates as a frequency divider.



Puls diagram / Impulsdiagramm

Moreover, this flip-flop has some more special features. When the signal changes from 0 -> 1 at the inputs J and K, ie when setting and resetting of flip-flops, it is irrelevant what signal (0 or 1) at the other input (stable) is present.
A full explanation of this circuit can be found in the article "Ideal pulse circuit without RC-combination and non-clocked JK flip-flops (http://www.klaus-e-schulz.de/dokumente/flipflop_en.pdf) ".
There you can find also a simple but very clear **simulation** of this circuit.

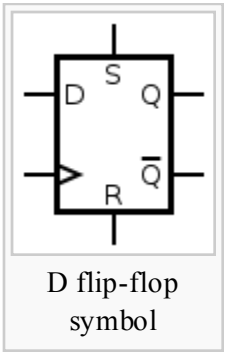


The basis for the function of this JK flip-flop is the novel realization of a pulse circuit (IIG).
The IIG has the following characteristics:
1. Only if input E changes its signal from 0 to 1, while the feedback R_m is 0, the output A will activated(0 -> 1)).
2. Immediately after receiving the feedback (R_m = 1) the output A will deactivated (0) again.

3. A signal change at R_m from 0 -> 1, during input E has 1-signal, the output A does **not** changes its state.
As result a puls with an optimal length was generated.

R_m is a feedback signal. Normally it is 0. It will be 1 when a triggered event - as result of the signal change from 0->1 at output A - has occurred.

D flip-flop



D flip-flop symbol

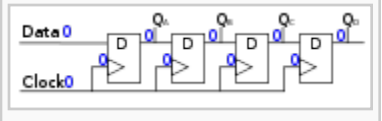
The D flip-flop is the most common flip-flop in use today. It is better known as *delay* flip-flop

The Q output always takes on the state of the D input at the moment of a positive edge (or negative edge if the clock input is active low).[7] It is called the **D** flip-flop for this reason, since the output takes the value of the **D** input or *Data* input, and *Delays* it by one clock count. The D flip-flop can be interpreted as a primitive memory cell, zero-order hold, or delay line. Whenever the clock pulses, the value of Q_{next} is D and Q_{prev} otherwise.

Truth table:

Clock	D	Q	Q_{prev}
Rising edge	0	0	X
Rising edge	1	1	X
Non-Rising	X	Q_{prev}	

('X' denotes a *Don't care* condition, meaning the signal is irrelevant)



4-bit serial-in, serial-out (SISO) shift register

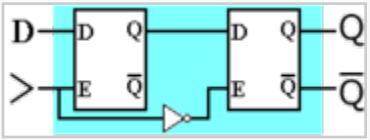
These flip-flops are very useful, as they form the basis for shift registers, which are an essential part of many electronic devices. The advantage of the D flip-flop over the D-type latch is that it "captures" the signal at the moment the clock goes high, and subsequent changes of the data line do not influence Q until the next rising clock edge. An exception is that some flip-flops have a "reset" signal input, which will reset Q (to zero), and may be either asynchronous or synchronous with the clock.

The above circuit shifts the contents of the register to the right, one bit position on each active transition of the clock. The input X is shifted into the leftmost bit position.

Master–slave (pulse-triggered) D flip-flop

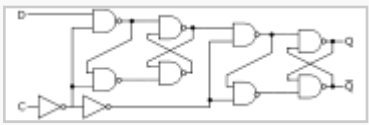
A master–slave D flip-flop is created by connecting two gated D latches in series, and inverting the *enable* input to one of them. It is called master–slave because the second latch in the series only changes in response to a change in the first (master) latch.

The term *pulse-triggered* means that data is entered on the rising edge of the clock pulse, but the output does not reflect the change until the falling edge of the clock pulse.



A master–slave D flip-flop. It responds on the negative edge of the *enable* input (usually a clock).

For a positive-edge triggered master–slave D flip-flop, when the clock signal is low (logical 0) the "enable" seen by the first or "master" D latch (the inverted clock signal) is high (logical 1). This allows the "master" latch to store the input value when the clock signal transitions from low to high. As the clock signal goes high (0 to 1) the inverted "enable" of the first latch goes low (1 to 0) and the value seen at the input to the master latch is "locked". Nearly simultaneously, the twice inverted "enable" of the second or "slave" D latch transitions from low to high (0 to 1) with the clock signal. This allows the signal captured at the rising edge of the clock by the now "locked" master latch to pass through the "slave" latch. When the clock signal returns to low (1 to 0), the output of the "slave" latch is "locked", and the value seen at the last rising edge of the clock is held while the "master" latch begins to accept new values in preparation for the next rising clock edge.

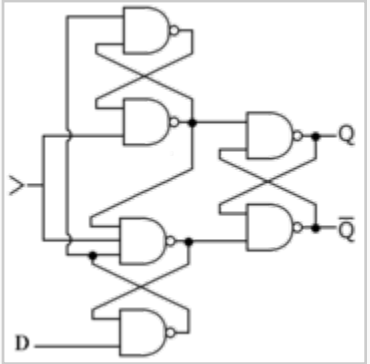

An implementation of a master–slave D flip-flop that is triggered on the positive edge of the clock

By removing the leftmost inverter in the above circuit, a D-type flip flop that strobes on the *falling edge* of a clock signal can be obtained. This has a truth table like this:

D	Q	>	Q_{next}
0	X	Falling	0
1	X	Falling	1

Most D-type flip-flops in ICs have the capability to be set and reset, much like an SR flip-flop. Usually, the illegal S = R = 1 condition is resolved in D-type flip-flops.

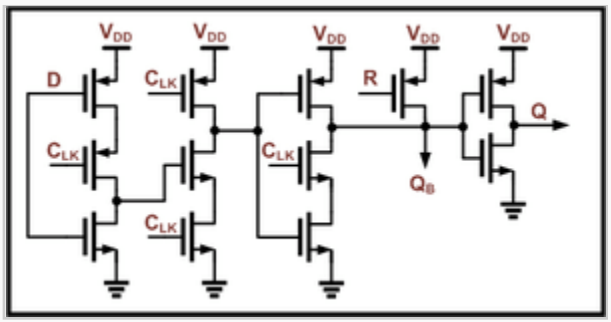
Inputs				Outputs	
S	R	D	>	Q	Q'
0	1	X	X	0	1
1	0	X	X	1	0
1	1	X	X	1	1



A positive-edge-triggered D flip-flop

By setting S = R = 0, the flip-flop can be used as described above.

Edge-triggered D flip-flop



A CMOS IC Implementation of a True Single Phase Edge Triggered Flip Flop with Reset

A more efficient way to make a D flip-flop is not so easy to understand, but it works the same way. While the master–slave D flip-flop is also triggered on the edge of a clock, its components are each triggered by clock levels. The "edge-triggered D flip-flop" does not have the master–slave properties.

Edge Triggered D flip flops are often implemented in integrated high speed operations using dynamic logic. This means that the digital output is stored on parasitic device capacitance while the device is not transitioning. This design of dynamic flip flops also enable simple resetting since the reset operation can be performed by simply discharging one or more internal nodes. A common dynamic flip flop variety is the True Single Phase Clock (TSPC) which performs the flip flop operation with little power and at high speeds.

Uses

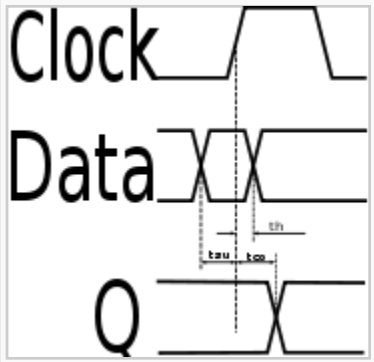
- A single flip-flop can be used to store one bit, or binary digit, of data. See preset.
- Any one of the flip-flop type can be used to build any of the others.
- Many logic synthesis tools will not use any other type than D flip-flop and D latch.
- Level sensitive latches cause problems with Static Timing Analysis (STA) tools and Design For Test (DFT). Therefore, their usage is often discouraged.
- Many FPGA devices contain only edge-triggered D flip-flops
- The data contained in several flip-flops may represent the state of a sequencer, the value of a counter, an ASCII character in a computer's memory or any other piece of information.
- One use is to build finite state machines from electronic logic. The flip-flops remember the machine's previous state, and digital logic uses that state to calculate the next state.
- The T flip-flop is useful for constructing various types of counters. Repeated signals to the clock input will cause the flip-flop to change state once per high-to-low transition of the clock input, if its T input is "1". The output from one flip-flop can be fed to the clock input of a second and so on. The final output of the circuit, considered as the array of outputs of all the individual flip-flops, is a count, in binary, of the number of cycles of the first clock input, up to a maximum of 2^n-1, where n is the number of flip-flops used. See: Counters
  - One of the problems with such a counter (called a *ripple counter*) is that the output is briefly invalid as the changes ripple through the logic. There are two solutions to this problem. The first is to sample the output only when it is known to be valid. The second, more widely used, is to use a different type of circuit called a *synchronous counter*. This uses more complex logic to ensure that the outputs of the counter all change at the same, predictable time. See: Counters
- Frequency division: a chain of T flip-flops as described above will also function to divide an input in frequency by 2^n, where n is the number of flip-flops used between the input and the output.

A flip-flop in combination with a Schmitt trigger can be used for the implementation of an arbiter in

asynchronous circuits.

Clocked flip-flops are prone to a problem called metastability, which happens when a data or control input is changing at the instant of the clock pulse. The result is that the output may behave unpredictably, taking many times longer than normal to settle to its correct state, or even oscillating several times before settling. Theoretically it can take infinite time to settle down. In a computer system this can cause corruption of data or a program crash.

The metastability in flip-flops can be avoided by ensuring that the data and control inputs are held valid and constant for specified periods before and after the clock pulse, called the **setup time** (t_{su}) and the **hold time** (t_h) respectively. These times are specified in the data sheet for the device, and are typically between a few nanoseconds and a few hundred picoseconds for modern devices.



Flip-flop setup, hold and clock-to-output timing parameters

Unfortunately, it is not always possible to meet the setup and hold criteria, because the flip-flop may be connected to a real-time signal that could change at any time, outside the control of the designer. In this case, the best the designer can do is to reduce the probability of error to a certain level, depending on the required reliability of the circuit. One technique for suppressing metastability is to connect two or more flip-flops in a chain, so that the output of each one feeds the data input of the next, and all devices share a common clock. With this method, the probability of a metastable event can be reduced to a negligible value, but never to zero. The probability of metastability gets closer and closer to zero as the number of flip-flops connected in series is increased.

So-called metastable-hardened flip-flops are available, which work by reducing the setup and hold times as much as possible, but even these cannot eliminate the problem entirely. This is because metastability is more than simply a matter of circuit design. When the transitions in the clock and the data are close together in time, the flip-flop is forced to decide which event happened first. However fast we make the device, there is always the possibility that the input events will be so close together that it cannot detect which one happened first. It is therefore logically impossible to build a perfectly metastable-proof flip-flop.

Another important timing value for a flip-flop (F/F) is the clock-to-output delay (common symbol in data sheets: t_{CO}) or propagation delay (t_P), which is the time the flip-flop takes to change its output after the clock edge. The time for a high-to-low transition (t_{PHL}) is sometimes different from the time for a low-to-high transition (t_{PLH}).

When cascading F/Fs which share the same clock (as in a shift register), it is important to ensure that the t_{CO} of a preceding F/F is longer than the hold time (t_h) of the following flip-flop, so data present at the input of the succeeding F/F is properly "shifted in" following the active edge of the clock. This relationship between t_{CO} and t_h is normally guaranteed if the F/Fs are physically identical. Furthermore, for correct operation, it is easy to verify that the clock period has to be greater than the sum $t_{su} + t_h$.

Chaos

Balthasar van der Pol was one of the first people to show electronic circuits may exhibit chaos in 1927, with the introduction of the Van der Pol oscillator. Then, Leon O. Chua showed circuits may exhibit chaos in 1983 through the introduction of Chua's circuit. Due to the qualitative nature of flip-flops, especially the Set/Reset Flip-Flop, one may intuitively feel it can exhibit chaos. This has been suggested in the works of Danca et al.[8]

and of Hamill et al.,[9] which discusses the qualitative nature of circuits:

> Voltages or currents may increase exponentially with time until limited, perhaps by power supply clipping, when the circuit may latch up. This type of instability is put to good use in circuits such as Schmitt triggers and flip-flops.[9]

and

> The waveforms may be noise like or chaotic, in which case they never repeat or latch up; as yet this type of behavior has few applications and is the least well understood.[9]

More recently in Blackmore et al.[10] it is shown that discrete models of the Set/Reset Flip-Flop can exhibit chaos.

Generalizations

Flip-flops can be generalized in at least two ways: by making them 1-of-N instead of 1-of-2, and by adapting them to logic with more than two states. In the special cases of 1-of-3 encoding, or multi-valued ternary logic, these elements may be referred to as *flip-flap-flops*.[11]

In a conventional flip-flop, exactly one of the two complementary outputs is high. This can be generalized to a memory element with N outputs, exactly one of which is high (alternatively, where exactly one of N is low). The output is therefore always a one-hot (respectively *one-cold*) representation. The construction is similar to a conventional cross-coupled flip-flop; each output, when high, inhibits all the other outputs.[12] Alternatively, more or less conventional flip-flops can be used, one per output, with additional circuitry to make sure only one at a time can be true.[13]

Another generalization of the conventional flip-flop is a memory element for multi-valued logic. In this case the memory element retains exactly one of the logic states until the control inputs induce a change.[14] In addition, a multiple-valued clock can also be used, leading to new possible clock transitions.[15]

Flip-flop integrated circuits

Integrated circuits (ICs) exist that provide one or more flip-flops. For example, the 7473 dual JK master–slave flip-flop, or the 74374 octal D flip-flop, in the 7400 series.

See also

- Astable
- Deadlock
- Monostable
- Pulse transition detector

Notes

1. ^ William Henry Eccles and Frank Wilfred Jordan, "Improvements in ionic relays (http://v3.espacenet.com/origdoc?DB=EPODOC&IDX=GB148582&F=0&QPN=GB148582) "

British patent number: GB 148582 (filed: 21 June 1918; published: 5 August 1920).
2. ^ W. H. Eccles and F. W. Jordan (19 September 1919) "A trigger relay utilizing three-electrode thermionic vacuum tubes," *The Electrician*, vol. 83, page 298. Reprinted in: *Radio Review*, vol. 1, no. 3, pages 143–146 (December 1919).
3. ^ Montgomery Phister (1958). *Logical Design of Digital Computers* (http://books.google.com/books?id=Ri1IAAAAIAAJ&q=inauthor:phister+j-k-flip-flop&dq=inauthor:phister+j-k-flip-flop&lr=&as_brr=0&as_pt=ALLTYPES&ei=8jfeSabSOZeSkASrm5naDQ&pgis=1) . Wiley. p. 128. http://books.google.com/books?id=Ri1IAAAAIAAJ&q=inauthor:phister+j-k-flip-flop&dq=inauthor:phister+j-k-flip-flop&lr=&as_brr=0&as_pt=ALLTYPES&ei=8jfeSabSOZeSkASrm5naDQ&pgis=1.
4. ^ Early master–slave devices actually remained (half) open between the first and second edge of a clocking pulse; today most flip-flops are designed so they may be clocked by a **single** edge as this gives large benefits regarding noise immunity, without any significant downsides.
5. ^ PHY107 Delay Flip-Flop (http://www.shef.ac.uk/physics/teaching/phy107/dff.html)
6. ^ ***a b c*** Mano, M. Morris; Kime, Charles R. (2004). *Logic and Computer Design Fundamentals, 3rd Edition*. Upper Saddle River, NJ, USA: Pearson Education International. pp. pg283. ISBN 0-13-1911651.
7. ^ The D Flip-Flop (http://www.play-hookey.com/digital/d_nand_flip-flop.html)
8. ^ Danca M-F. (2008). "Numerical approximation of a class of switch dynamical systems". *Chaos, Solitons and Fractals* **38**: 184–191. doi:10.1016/j.chaos.2006.11.003 (http://dx.doi.org/10.1016%2Fj.chaos.2006.11.003) .
9. ^ Hamill D, Deane J, Jeffries D (1992). "Modeling of chaotic DC/DC converters by iterated nonlinear maps". *IEEE Trans Power Electronics* **7**: 25–36. doi:10.1109/63.124574 (http://dx.doi.org/10.1109%2F63.124574) .
10. ^ Blackmore, D, Rahman, A, Shah, J (2009). "Discrete dynamical modeling and analysis of the R–S flip-flop circuit". *Chaos, Solitons and Fractals* **42**: 951. doi:10.1016/j.chaos.2009.02.032 (http://dx.doi.org/10.1016%2Fj.chaos.2009.02.032) .
11. ^ Often attributed to Don Knuth (1969) (see Midhat J. Gazalé (2000). *Number: from Ahmes to Cantor* (http://books.google.com/books?id=hARkwMkeliUC&pg=PA57&dq=flip-flap-flop+knuth&lr=&as_brr=0&ei=RQHaSry9NoLskQTlzYyFAQ#v=onepage&q=flip-flap-flop%20knuth&f=false) . Princeton University Press. p. 57. ISBN 9780691005157. http://books.google.com/books?id=hARkwMkeliUC&pg=PA57&dq=flip-flap-flop+knuth&lr=&as_brr=0&ei=RQHaSry9NoLskQTlzYyFAQ#v=onepage&q=flip-flap-flop%20knuth&f=false.), the term *flip-flap-flop* actually appeared much earlier in the computing literature, for example, Edward K. Bowdon (1960). *The design and application of a "flip-flap-flop" using tunnel diodes (Master's thesis)* (http://books.google.com/books?id=0pA7AAAAMAAJ&q=flip-flap-flop+core&dq=flip-flap-flop+core&lr=&as_brr=0&ei=OwPaSvKpPJaGkATR_YD8BQ) . University of North Dakota. http://books.google.com/books?id=0pA7AAAAMAAJ&q=flip-flap-flop+core&dq=flip-flap-flop+core&lr=&as_brr=0&ei=OwPaSvKpPJaGkATR_YD8BQ.
12. ^ "Ternary "flip-flap-flop"" (http://www.goldenmuseum.com/1411FlipFlap_engl.html) . http://www.goldenmuseum.com/1411FlipFlap_engl.html.
13. ^ US patent 6975152 (http://v3.espacenet.com/textdoc?DB=EPODOC&IDX=US6975152)
14. ^ Irving, Thurman A. and Shiva, Sajjan G. and Nagle, H. Troy (March 1976). "Flip-Flops for Multiple-Valued Logic". *Computers, IEEE Transactions on* **C-25** (3): pp. 237–246. doi:10.1109/TC.1976.5009250 (http://dx.doi.org/10.1109%2FTC.1976.5009250) .
15. ^ Wu Haomin1 and Zhuang Nan2. "Research into ternary edge-triggered JKL flip-flop". *Journal of Electronics (China)* (Volume 8, Number 3 / July, 1991): pp. 268–275. doi:10.1007/BF02778378 (http://dx.doi.org/10.1007%2FBF02778378) .

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- Salman, E., Dasdan, A., Taraporevala, F., Kucukcakar, K., Friedman, E. (2006). "Pessimism Reduction in Static Timing Analysis Using Interdependent Setup and Hold Times". Proc. of Int. Symp. on Quality Electronic Design (ISQED). pp. 159–164. (This paper explains the interdependence of setup time, hold time, and clock-to-q delay and shows how to use it for pessimism reduction in static timing analysis.)
- Schulz, Klaus-E. (2007). Ideal pulse circuit without RC-combination and non-clocked JK flip-flops (look discussion) (http://www.hpc-berlin.de/dokumente/flipflop_en.pdf)
- Keating, M., Bricaud, P. (2002). *ReuseMethodology Manual*. KAP. ISBN 1-4020-7141-4.

Categories: Digital electronics | Electronic engineering | Digital systems | Oscillators | Logic gates

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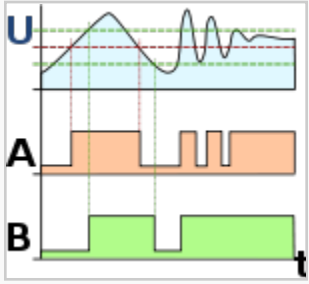
Schmitt trigger

From Wikipedia, the free encyclopedia

In electronics, a **Schmitt trigger** is a comparator circuit that incorporates positive feedback.

When the input is higher than a certain chosen threshold, the output is high; when the input is below another (lower) chosen threshold, the output is low; when the input is between the two, the output retains its value. The trigger is so named because the output retains its value until the input changes sufficiently to trigger a change. This dual threshold action is called *hysteresis*, and implies that the Schmitt trigger has some memory. In fact, the Schmitt trigger is a bistable multivibrator.

Schmitt trigger devices are typically used in open loop configurations for noise immunity and closed loop positive feedback configurations to implement multivibrators.



The effect of using a Schmitt trigger (B) instead of a comparator (A).

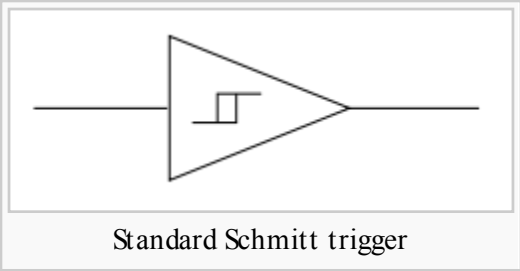
Contents

Invention

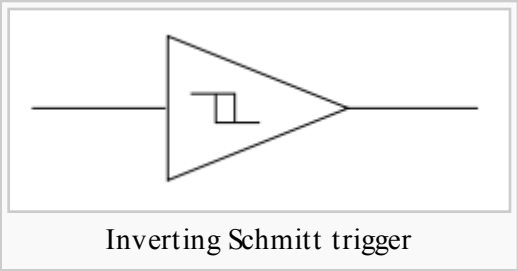
The Schmitt trigger was invented by US scientist Otto H. Schmitt in 1934 while he was still a graduate student,[1] later described in his doctoral dissertation (1937) as a "thermionic trigger".[2] It was a direct result of Schmitt's study of the neural impulse propagation in squid nerves.[2]

Symbol

The symbol for Schmitt triggers in circuit diagrams is a triangle with an inverting or non-inverting hysteresis symbol. The symbol depicts the corresponding ideal hysteresis curve.



Standard Schmitt trigger



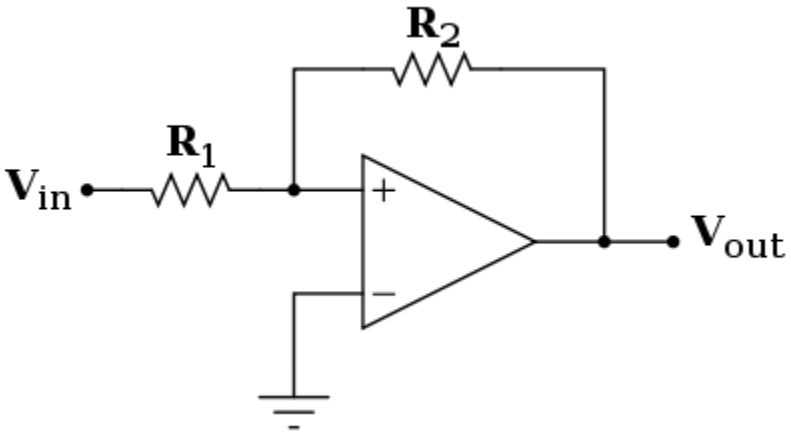
Inverting Schmitt trigger

Implementation

A Schmitt trigger can be implemented with a simple tunnel diode, a diode with an "N"-shaped current–voltage characteristic in the first quadrant. An oscillating input will cause the diode to move from one rising leg of the "N" to the other and back again as the input crosses the rising and falling switching thresholds. However, the performance of this Schmitt trigger can be improved with transistor-based devices that make explicit use of positive feedback to implement the switching.

Comparator implementation

Schmitt triggers are commonly implemented using a comparator[nb 1] connected to have positive feedback (i.e., instead of the usual negative feedback used in operational amplifier circuits). For this circuit, the switching occurs near ground, with the amount of hysteresis controlled by the resistances of R_1 and R_2:



The comparator extracts the sign of the difference between its two inputs. When the non-inverting (+) input is at a higher voltage than the inverting (-) input, the comparator output switches to $+V_S$, which is its high supply voltage. When the non-inverting (+) input is at a lower voltage than the inverting (-) input, the comparator output switches to $-V_S$, which is its low supply voltage. In this case, the inverting (-) input is grounded, and so the comparator implements the sign function – its 2-state output (i.e., either high or low) always has the same sign as the continuous input at its non-inverting (+) terminal.

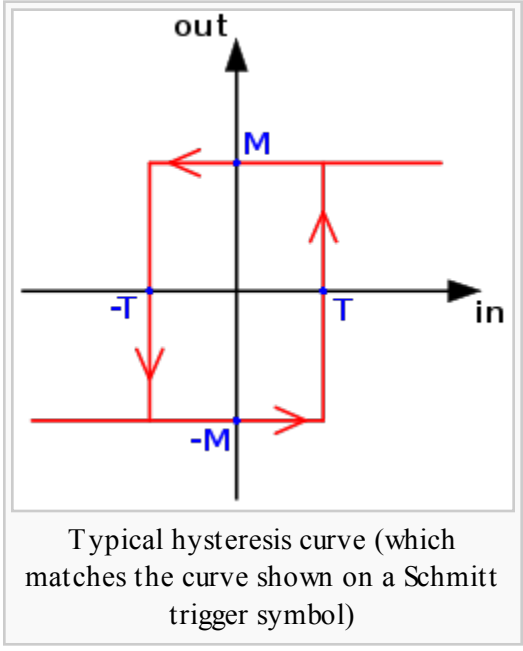
Because of the resistor network connecting the Schmitt trigger input, the non-inverting (+) terminal of the comparator, and the comparator output, the Schmitt trigger acts like a comparator that switches at a different point depending on whether the output of the comparator is high or low. For very negative inputs, the output will be low, and for very positive inputs, the output will be high, and so this is an implementation of a

"non-inverting" Schmitt trigger. However, for intermediate inputs, the state of the output depends on both the input and the output. For instance, if the Schmitt trigger is currently in the high state, the output will be at the positive power supply rail (+V_S). V_+ is then a voltage divider between V_{in} and +V_S. The comparator will switch when V_+=0 (ground). Current conservation shows that this requires

$$\frac{V_{\text{in}}}{R_1} = -\frac{V_S}{R_2}$$

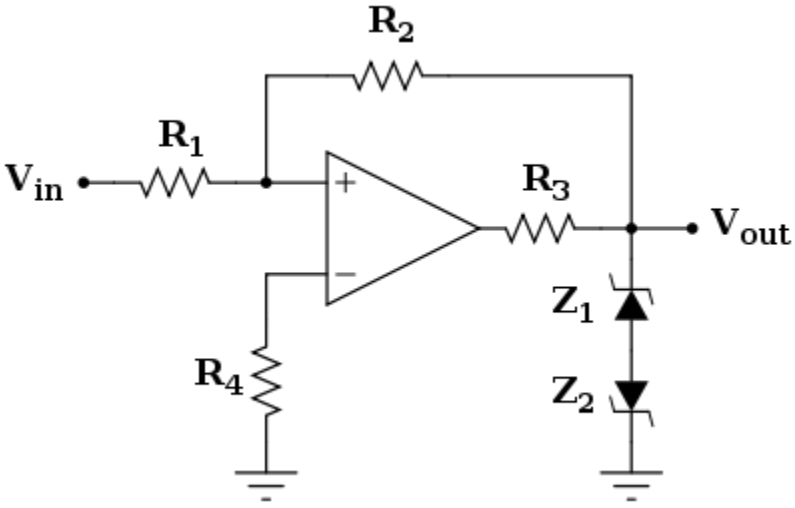
and so V_{in} must drop below $-\frac{R_1}{R_2}V_s$ to get the output to switch. Once the comparator output has switched to $-V_S$, the threshold becomes $+\frac{R_1}{R_2}V_s$ to switch back to high.

So this circuit creates a switching band centered around zero, with trigger levels $\pm\frac{R_1}{R_2}V_s$. The input voltage must rise above the top of the band, and then below the bottom of the band, for the output to switch on and then back off. If R_1 is zero or R_2 is infinity (i.e., an open circuit), the band collapses to zero width, and it behaves as a standard comparator. The output characteristic is shown in the picture on the right. The value of the threshold T is given by $\frac{R_1}{R_2}V_s$ and the maximum value of the output M is the power supply rail.



Typical hysteresis curve (which matches the curve shown on a Schmitt trigger symbol)

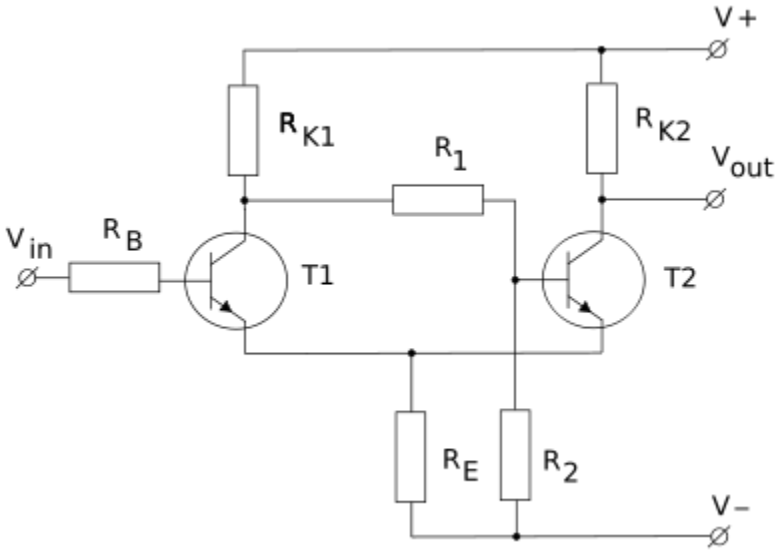
A practical Schmitt trigger configuration is shown below.



The output characteristic has exactly the same shape of the previous basic configuration, and the threshold values are the same as well. On the other hand, in the previous case, the output voltage was depending on the power supply, while now it is defined by the Zener diodes (which could also be replaced with a single double-anode Zener diode). In this configuration, the output levels can be modified by appropriate choice of Zener diode, and these levels are resistant to power supply fluctuations (i.e., they increase the PSRR of the comparator). The resistor R_3 is there to limit the current through the diodes, and the resistor R_4 minimizes the input voltage offset caused by the comparator's input leakage currents (see *Limitations of real op-amps*).

Schmitt trigger with two transistors

In the positive-feedback configuration used in the implementation of a Schmitt trigger, most of the complexity of the comparator's own implementation is unused. Hence, it can be replaced with two cross-coupled transistors (i.e., the transistors that would otherwise implement the input stage of the comparator). An example of such a 2-transistor-based configuration is shown below. The chain R_{K1} R_1 R_2 sets the base voltage for transistor T2. This divider, however, is affected by transistor T1, providing higher voltage if T1 is open. Hence the threshold voltage for switching between the states depends on the present state of the trigger.



For NPN transistors as shown, when the input voltage is well below the shared emitter voltage, T1 does not conduct. The base voltage of transistor T2 is determined by the mentioned divider. Due to negative feedback, the voltage at the shared emitters must be almost as high as that set by the divider so that T2 is conducting, and the trigger output is in the low state. T1 will conduct when the input voltage (T1 base voltage) rises slightly above the voltage across resistor R_E (emitter voltage). When T1 begins to conduct, T2 ceases to conduct, because the voltage divider now provides lower T2 base voltage while the emitter voltage does not drop because T1 is now drawing current across R_E. With T2 now not conducting the trigger has transitioned to the high state.

With the trigger now in the high state, if the input voltage lowers enough, the current through T1 reduces, lowering the shared emitter voltage and raising the base voltage for T2. As T2 begins to conduct, the voltage across R_E rises, further reducing the T1 base-emitter potential and T1 ceases to conduct.

In the high state, the output voltage is close to V+, but in the low state it is still well above V−. This may not be low enough to be a "logical zero " for digital circuits. This may require additional amplifiers following the trigger circuit.

The circuit can be simplified: R1 can be omitted, connecting the T2 base directly to the T1 collector, and the connection of the T2 base to V- via R2 can be completely omitted. When T1 conducts, it connects the T2 base to the T2 emitter so that T2 does not conduct. When T1 does not conduct, R_{K1} pulls up the T2 base and T2 conducts.

Applications

Schmitt triggers are typically used in open loop configurations for noise immunity and closed loop positive feedback configurations to implement multivibrators.

Noise immunity

One application of a Schmitt trigger is to increase the noise immunity in a circuit with only a single input threshold. With only one input threshold, a noisy input signal near that threshold could cause the output to switch rapidly back and forth from noise alone. A noisy Schmitt Trigger input signal near one threshold can cause only one switch in output value, after which it would have to move beyond the other threshold in order to cause another switch.

For example, in Fairchild Semiconductor's QSE15x family of infrared photosensors[3], an amplified infrared photodiode generates an electric signal that switches frequently between its absolute lowest value and its absolute highest value. This signal is then low-pass filtered to form a smooth signal that rises and falls corresponding to the relative amount of time the switching signal is on and off. That filtered output passes to the input of a Schmitt trigger. The net effect is that the output of the Schmitt trigger only passes from low to high after a received infrared signal excites the photodiode for longer than some known delay, and once the Schmitt trigger is high, it only moves low after the infrared signal ceases to excite the photodiode for longer than a similar known delay. Whereas the photodiode is prone to spurious switching due to noise from the environment, the delay added by the filter and Schmitt trigger ensures that the output only switches when there is certainly an input stimulating the device.

Devices that include a built-in Schmitt trigger

As discussed in the example above, the Fairchild Semiconductor QSE15x family of photosensors use a Schmitt trigger internally for noise immunity. Schmitt triggers are common in many switching circuits for similar reasons (e.g., for switch debouncing).

The following 7400 series devices include a Schmitt trigger on their input or on each of their inputs:

- 7413: Dual Schmitt trigger 4-input NAND Gate
- 7414: Hex Schmitt trigger Inverter
- 7419: Hex Schmitt trigger Inverter
- 74121: Monostable Multivibrator with Schmitt Trigger Inputs
- 74132: Quad 2-input NAND Schmitt Trigger
- 74221: Dual Monostable Multivibrator with Schmitt Trigger Input
- 74232: Quad NOR Schmitt Trigger
- 74240: Octal Buffer with Schmitt Trigger Inputs and Three-State Inverted Outputs
- 74241: Octal Buffer with Schmitt Trigger Inputs and Three-State Noninverted Outputs
- 74244: Octal Buffer with Schmitt Trigger Inputs and Three-State Noninverted Outputs
- 74310: Octal Buffer with Schmitt Trigger Inputs
- 74540: Octal Buffer with Schmitt Trigger Inputs and Three-State Inverted Outputs
- 74541: Octal Buffer with Schmitt Trigger Inputs and Three-State Noninverted Outputs

A number of 4000 series devices include a Schmitt trigger on inputs, for example:

- 14093: Quad 2-Input NAND
- 40106: Hex Inverter
- 14538: Dual Monostable Multivibrator
- 4020: 14-Stage Binary Ripple Counter
- 4024: 7-Stage Binary Ripple Counter

- 4040: 12-Stage Binary Ripple Counter
- 4017: Decade Counter with Decoded Outputs
- 4022: Octal Counter with Decoded Outputs
- 4093: Quad Dual Input NAND gate

Dual Schmitt input configurable single-gate CMOS logic, AND, OR, XOR, NAND, NOR, XNOR

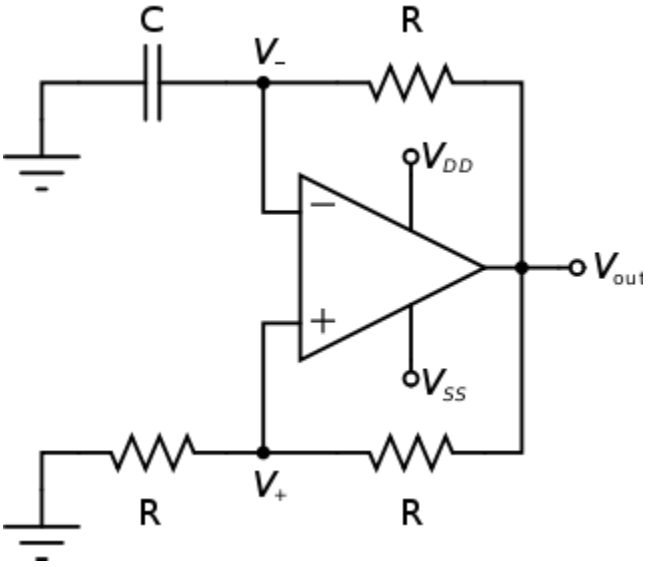
- NC7SZ57 Fairchild
- NC7SZ58 Fairchild
- SN74LVC1G57 Texas Instruments
- SN74LVC1G58 Texas Instruments

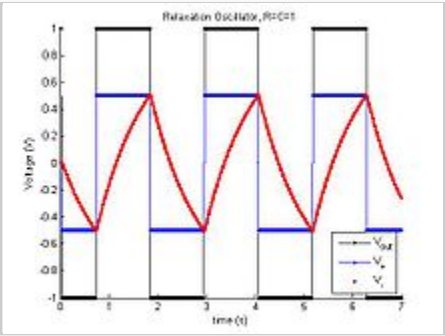
Use as an oscillator

Main article: Relaxation oscillator

A Schmitt trigger is a bistable multivibrator, and it can be used to implement another type of multivibrator, the relaxation oscillator. This is achieved by connecting a single resistor–capacitor network to an inverting Schmitt trigger – the capacitor connects between the input and ground and the resistor connects between the output and the input. The output will be a continuous square wave whose frequency depends on the values of R and C, and the threshold points of the Schmitt trigger. Since multiple Schmitt trigger circuits can be provided by a single integrated circuit (e.g. the 4000 series CMOS device type 40106 contains 6 of them), a spare section of the IC can be quickly pressed into service as a simple and reliable oscillator with only two external components.

For example, the comparator-based implementation of a relaxation oscillator is shown below.





Output and capacitor waveforms for comparator-based relaxation oscillator.

Here, a comparator-based Schmitt trigger is used in its inverting configuration. That is, the input and ground are swapped from the Schmitt trigger shown above, and so very negative signals correspond to a positive output and very positive signals correspond to a negative output. Additionally, slow negative feedback is added with an RC network. The result, which is shown on the right, is that the output automatically oscillates from V_{SS} to V_{DD} as the capacitor charges from one Schmitt trigger threshold to the other.

See also

- oscillator
- Bistable multivibrator

Notes

1. ^ Operational amplifiers sometimes may be used to implement comparators. However, many operational amplifiers are designed to be used only in negative-feedback configurations that enforce a negligible difference between the inverting and non-inverting inputs. Some operational amplifiers incorporate input-protection circuitry that prevent the inverting and non-inverting inputs from operating far away from each other. For example, clipper circuits made up of two general purpose diodes with opposite bias in parallel or two Zener diodes with opposite bias in series (i.e., a double-anode Zener diode) are sometimes used internally across the two inputs of the operational amplifier.[*citation needed*] In these cases, the operational amplifiers will fail to function well as comparators. Conversely, comparators are designed under the assumption that the input voltages can differ significantly.

References

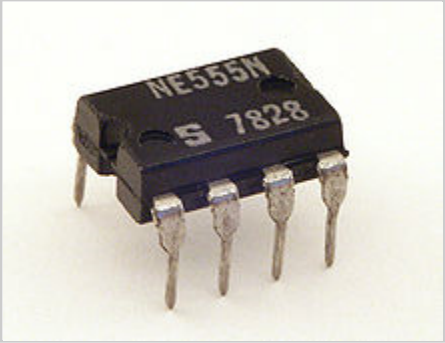
1. ^ Otto H. Schmitt, A Thermionic Trigger (http://dx.doi.org/10.1088/0950-7671/15/1/305) , Journal of Scientific Instruments 15 (January 1938): 24–26.
2. ^ ***a b*** August 2004 issue of the Pavek Museum of Broadcasting Newsletter - http://www.otto-schmitt.org/Otto_Images/PavekOHSbio.pdf
3. ^ Fairchild Semiconductor QSE15x photosensors: Product page (http://www.fairchildsemi.com/pf/QS/QSE158.html) , Datasheet (http://www.fairchildsemi.com/ds/QS/QSE158.pdf)

External links

- Hyperphysics description and equations for an alternative, more general circuit (http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/schmitt.html)
- Calculator which determines the resistor values required for given thresholds (http://www.random-science-tools.com/electronics/schmitt-trigger-calculator.htm)

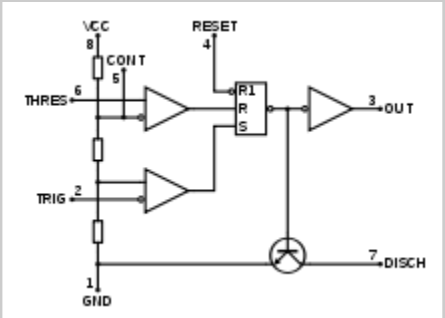
555 timer IC

From Wikipedia, the free encyclopedia



NE555 from Signetics in dual-in-line package

The **555 Timer IC** is an integrated circuit (chip) implementing a variety of timer and multivibrator applications. The IC was designed by Hans R. Camenzind in 1970 and brought to market in 1971 by Signetics (later acquired by Philips). The original name was the SE555 (metal can)/**NE555** (plastic DIP) and the part was described as "The IC Time Machine"[1]. It has been claimed that the 555 gets its name from the three 5 kΩ resistors used in typical early implementations,[2] but Hanz Camenzind has stated that the number was arbitrary[3]. The part is still in wide use, thanks to its ease of use, low price and good stability. As of 2003, it is estimated that 1 billion units are manufactured every year[3].



Internal block diagram

Depending on the manufacturer, the standard 555 package includes over 20 transistors, 2 diodes and 15 resistors on a silicon chip installed in an 8-pin mini dual-in-line package (DIP-8).[4] Variants available include the 556 (a 14-pin DIP combining two 555s on one chip), and the 558 (a 16-pin DIP combining four slightly modified 555s with DIS & THR connected internally, and TR falling edge sensitive instead of level sensitive).

Ultra-low power versions of the 555 are also available, such as the 7555 and TLC555.[5] The 7555 requires slightly different wiring using fewer external components and less power.

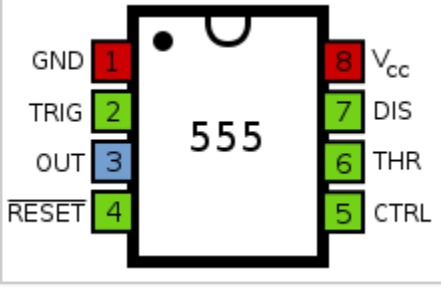
The 555 has three operating modes:

- Monostable mode: in this mode, the 555 functions as a "one-shot". Applications include timers, missing pulse detection, bouncefree switches, touch switches, frequency divider, capacitance measurement, pulse-width modulation (PWM) etc
- Astable - free running mode: the 555 can operate as an oscillator. Uses include LED and lamp flashers, pulse generation, logic clocks, tone generation, security alarms, pulse position modulation, etc.
- Bistable mode or Schmitt trigger: the 555 can operate as a flip-flop, if the DIS pin is not connected and no capacitor is used. Uses include bouncefree latched switches, etc.

Contents

Usage

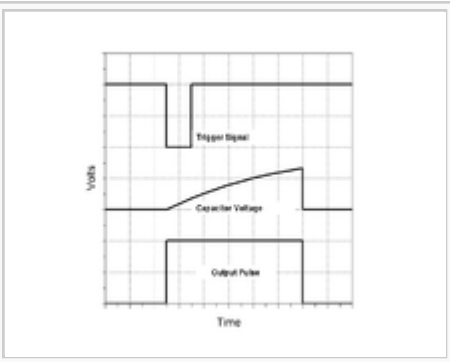
The connection of the pins is as follows:



Schematic symbol

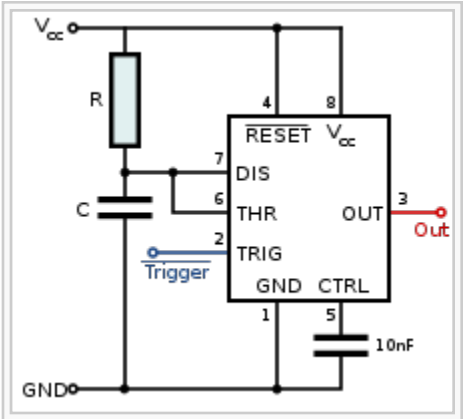
Nr.	Name	Purpose
1	GND	Ground, low level (0 V)
2	TRIG	A short pulse high-to-low on the trigger starts the timer
3	OUT	During a timing interval, the output stays at $+V_{CC}$
4	$\overline{\text{RESET}}$	A timing interval can be interrupted by applying a reset pulse to low (0 V)
5	CTRL	Control voltage allows access to the internal voltage divider (2/3 V_{CC})
6	THR	The threshold at which the interval ends (it ends if the voltage at THR is at least 2/3 V_{CC})
7	DIS	Connected to a capacitor whose discharge time will influence the timing interval
8	$V+$, V_{CC}	The positive supply voltage which must be between 3 and 15 V

Monostable mode



The relationships of the trigger signal, the voltage on C and the pulse width in monostable mode

In the monostable mode, the 555 timer acts as a "one-shot" pulse generator. The pulse begins when the 555 timer receives a trigger signal. The width of the pulse is determined by the time constant of an RC network, which consists of a capacitor (C) and a resistor (R). The pulse ends when the charge on the C equals 2/3 of the supply voltage. The pulse width can be lengthened or shortened to the need of the specific application by adjusting the values of R and C.[6]



Schematic of a 555 in monostable mode

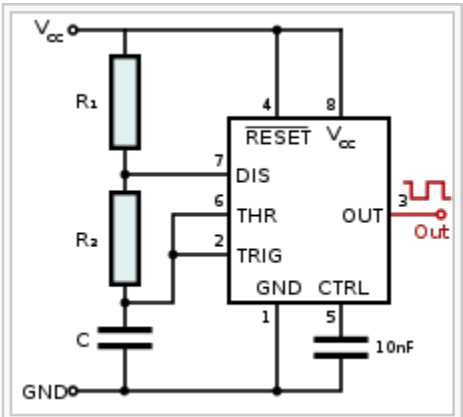
The pulse width of time *t*, which is the time it takes to charge C to 2/3 of the supply voltage, is given by

$$t = RC\ln(3) \approx 1.1RC$$

where t is in seconds, R is in ohms and C is in farads. See RC circuit for an explanation of this effect.

Astable mode

In astable mode, the '555 timer' puts out a continuous stream of rectangular pulses having a specified frequency. Resistor R_1 is connected between V_{CC} and the discharge pin (pin 7) and another resistor (R_2) is connected between the discharge pin (pin 7), and the trigger (pin 2) and threshold (pin 6) pins that share a common node. Hence the capacitor is charged through R_1 and R_2, and discharged only through R_2, since pin 7 has low impedance to ground during output low intervals of the cycle, therefore discharging the capacitor.



Standard 555 Astable Circuit

In the astable mode, the frequency of the pulse stream depends on the values of R_1, R_2 and C:

$$f = \frac{1}{(\ln(2)\cdot C\cdot(R_1+2R_2))}$$ [7]

The high time from each pulse is given by

$$high = \ln(2)\cdot(R_1+R_2)\cdot C$$

and the low time from each pulse is given by

$$low = \ln(2)\cdot R_2\cdot C$$

where R_1 and R_2 are the values of the resistors in ohms and C is the value of the capacitor in farads.

Specifications

These specifications apply to the NE555. Other 555 timers can have better specifications depending on the grade (military, medical, etc).

Supply voltage (V_{CC})	4.5 to 15 V
Supply current (V_{CC} = +5 V)	3 to 6 mA
Supply current (V_{CC} = +15 V)	10 to 15 mA
Output current (maximum)	200 mA
Power dissipation	600 mW
Operating temperature	0 to 70 °C

Derivatives

Many pin-compatible variants, including CMOS versions, have been built by various companies. Bigger packages also exist with two or four timers on the same chip. The 555 is also known under the following type numbers:

Manufacturer	Model	Remark
Custom Silicon Solutions (http://www.customsiliconsolutions.com)	CSS555/CSS555C	CMOS from 1.2 V, IDD < 5 µA
ECG Philips	ECG955M	
Exar	XR-555	
Fairchild Semiconductor	NE555/KA555	
Harris	HA555	
IK Semicon	ILC555	CMOS from 2 V
Intersil	SE555/NE555/ICM7555	
Lithic Systems	LC555	
Maxim	ICM7555	CMOS from 2 V
Motorola	MC1455/MC1555	
National Semiconductor	LM1455/LM555 /LM555C	
National Semiconductor	LMC555	CMOS from 1.5 V
NTE Sylvania	NTE955M	
Raytheon	RM555/RC555	

RCA	CA555/CA555C	
STMicroelectronics	NE555N/ K3T647	
Texas Instruments	SN52555/SN72555; TLC555	latter: CMOS from 2 V
USSR	К1006ВИ1	
Zetex	ZSCT1555	down to 0.9 V

Dual timer 556

The dual version is called 556. It features two complete 555s in a 14 pin DIL package.

Quad timer 558

The quad version is called 558 and has 16 pins. To fit four 555's into a 16 pin package the control voltage and reset lines are shared by all four modules. Also for each module the discharge and threshold are internally wired together and called *timing*.

Example applications

Joystick interface circuit using quad timer 558

The original IBM personal computer used a quad timer 558 in monostable (or "one-shot") mode to interface up to two joysticks to the host computer.[8] In the joystick interface circuit of the IBM PC, the capacitor (C) of the RC network (see Monostable Mode above) was generally a 10 nF capacitor. The resistor (R) of the RC network consisted of the potentiometer inside the joystick along with an external resistor of 2.2 kilohms.[9] The joystick potentiometer acted as a variable resistor. By moving the joystick, the resistance of the joystick increased from a small value up to about 100 kilohms. The joystick operated at 5 V.[10]

Software running in the host computer started the process of determining the joystick position by writing to a special address (ISA bus I/O address 201h).[11][12] This would result in a trigger signal to the quad timer, which would cause the capacitor (C) of the RC network to begin charging and cause the quad timer to output a pulse. The width of the pulse was determined by how long it took the C to charge up to 2/3 of 5 V (or about 3.33 V), which was in turn determined by the joystick position.[13][14]

Software running in the host computer measured the pulse width to determine the joystick position. A wide pulse represented the full-right joystick position, for example, while a narrow pulse represented the full-left joystick position.[10]

References

1. ^ van Roon, Tony, "555 Timer Tutorial," p. 1.
2. ^ Scherz, Paul, "Practical Electronics for Inventors," p. 589.
3. ^ *a b* |THE 555 TIMER IC - An Interview with Hans Camenzind (http://www.semiconductormuseum.com

/Transistors/LectureHall/Camenzind/Camenzind_Page2.htm)
4. ^ van Roon, Tony, "555 Timer Tutorial," Fig. 3 and related text.
5. ^ Jung, Walter G., "IC Timer Cookbook, Second Edition," pp. 40–41.
6. ^ van Roon, Tony, "555 Timer Tutorial," at "Monostable Mode"
7. ^ van Roon, Tony, "555 Timer Tutorial," at "Astable operation"
8. ^ Engdahl, Tomi. "PC analogue joystick interface, Introduction" (http://www.epanorama.net/documents/joystick/pc_joystick.html) . http://www.epanorama.net/documents/joystick/pc_joystick.html. Retrieved 2009-06-06.
9. ^ Engdahl, Tomi, "PC analogue joystick interface," at "Circuit diagram of PC joystick interface"
10. ^ ***a b*** Engdahl, Tomi, "PC analogue joystick interface," at "Joystick construction"
11. ^ Engdahl, Tomi, "PC analogue joystick interface," at "How PC joystick port hardware works"
12. ^ Eggebrecht, Lewis C., "Interfacing to the IBM Personal Computer," at p. 197
13. ^ Engdahl, Tomi, "PC analogue joystick interface," at "Introduction" and "Resistive analogue inputs (joystick position)"
14. ^ Eggebrecht, Lewis C., "Interfacing to the IBM Personal Computer," at pp. 197-99

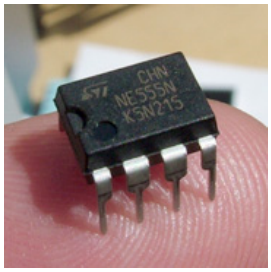
External links

- Data Sheet (Custom Silicon Solutions) (PDF) (http://www.customsiliconsolutions.com/products-for-ASIC-solutions/standard-IC-products_no.aspx)
- 555 Timer Circuits - the Astable, Monostable and Bistable (http://www.eleinmec.com/article.asp?1)
- 555 and 556 Timer Circuits (http://www.kpsec.freeuk.com/555timer.htm)
- 555 Timer Pin configurations (http://www.world-class-programme.com/555-Timer.asp)
- Data Sheet (Fairchild) (PDF) (http://www.fairchildsemi.com/ds/LM%2FLM555.pdf)
- Java simulation (http://www.falstad.com/circuit/e-555square.html) of 555 oscillator circuit
- 1972 Signetics NE555 datasheet (PDF) (http://www.datasheetarchive.com/search.php?q=NE555&sType=part&ExactDS=Starts)
- 555 timer info (http://www.doctronics.co.uk/555.htm)
- Frequency, and pulse time calculator (http://utilitymill.com/utility/Astable_mode_555_timer_frequency_calculator)
- Using NE 555 as a Temperature DSP (http://www.globu.net/pp/english/pp/ne555.htm)
- Frequency and duty cycle calculator for astable multivibrators based on the NE555 (http://www.daycounter.com/Calculators/NE555-Calculator.phtml)
- How to build a (http://www.instructables.com/id/SORIJ3MFAQDX2PW/) camera intervalometer using a 555

555 Timer

The web's favourite 555 timer resource (*Google* top!) just got better...

Navigation



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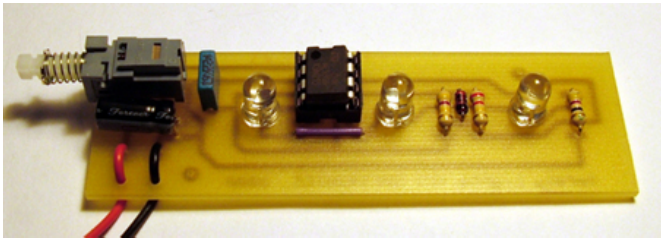
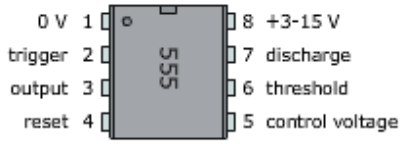
Learn about the 555 by building the DOCTRONICS Safety Lights Project:



DOCTRONICS Safety Lights construction kit

1. Pin connections



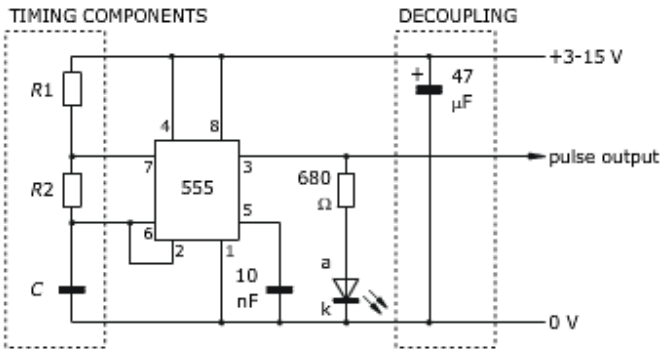
555 timer pin connections

The 555 timer is an extremely versatile integrated circuit which can be used to build lots of different circuits. You can use the 555 effectively without understanding the function of each pin in detail.

Frequently, the 555 is used in astable mode to generate a continuous series of pulses, but you can also use the 555 to make a one-shot or monostable circuit. The 555 can source or sink 200 mA of output current, and is capable of driving wide range of output devices.

2. Astable circuits

Astable circuits produce pulses. The circuit most people use to make a 555 astable looks like this:



555 astable circuit

The button allows you to open a simulation of this circuit in *Yenka©*, the new electronics simulation program from *Crocodile Clips Limited*. To use the program, you need to download and install the *Yenka©* plug-in.

At the moment, *Yenka* is available for free download to home users from http://www.yenka.com/. This is a fantastic offer from the creators of *Yenka©*: don't miss it!

As you can see, the frequency, or repetition rate, of the output pulses is determined by the values of two resistors, *R*1 and *R*2 and by the timing capacitor, *C*.

The design formula for the frequency of the pulses is:

$$f = \frac{1.44}{(R1 + 2R2) \times C}$$

The period, *t*, of the pulses is given by:

$$t = \frac{1}{f} = 0.69(R1 + 2R2) \times C$$

The HIGH and LOW times of each pulse can be calculated from:

$$\text{HIGH time} = 0.69(R1 + R2) \times C$$ $$\text{LOW time} = 0.69(R2 \times C)$$

The duty cycle of the waveform, usually expressed as a percentage, is given by:

$$\text{duty cycle} = \frac{\text{HIGH time}}{\text{pulse period time}}$$

An alternative measurement of HIGH and LOW times is the mark space ratio:

$$\text{mark space ratio} = \frac{\text{HIGH time}}{\text{LOW time}}$$

Before calculating a frequency, you should know that it is usual to make $R1$=1 kΩ because this helps to give the output pulses a duty cycle close to 50%, that is, the HIGH and LOW times of the pulses are approximately equal.

Remember that design formulae work in fundamental units. However, it is often more convenient to work with other combinations of units:

resistance	*capacitance*	*period*	*frequency*
Ω	F	s	Hz
MΩ	μF	s	Hz
kΩ	μF	ms	kHz

With R values in MΩ and C values in μF, the frequency will be in Hz. Alternatively, with R values in kΩ and C values in μF, frequencies will be in kHz.

Suppose you want to design a circuit to produce a frequency of approximately 1 kHz for an alarm application. What values of $R1$, $R2$ and C should you use?

$R1$ should be 1kΩ, as already explained. This leaves you with the task of selecting values for $R2$ and C. The best thing to do is to rearrange the design formula so that the R values are on the right hand side:

$$R1 + 2R2 = \frac{1.44}{f \times C}$$

Now substitute for $R1$ and f :

$$1 + 2R2 = \frac{1.44}{1 \times C}$$

You are using R values in kΩ and f values in kHz, so C values will be in μF.

To make further progress, you must choose a value for C. At the same time, it is important to remember that practical values for $R2$ are between 1 kΩ and 1MΩ. Suppose you choose C = 10 nF = 0.01 μF:

$$1 + 2R2 = \frac{1.44}{0.01} = 144$$

That is:

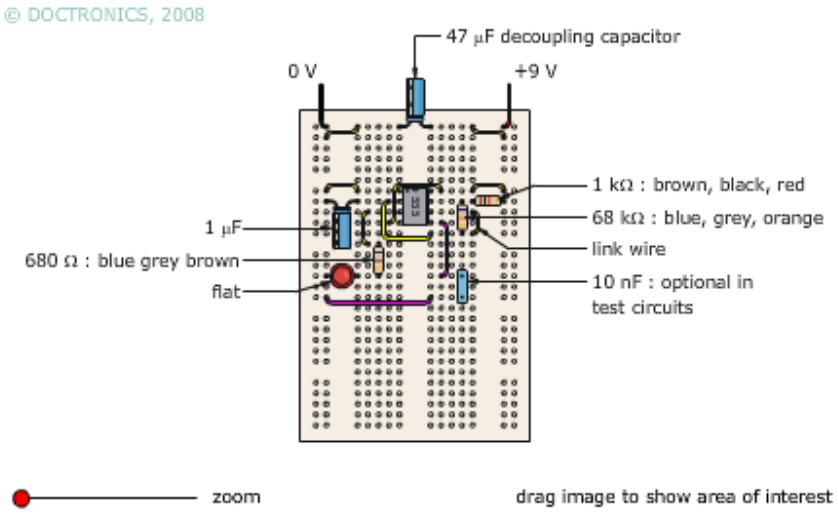
$$2R2 = 144 - 1 = 143$$

and:

$$R2 = 71.5\,\text{k}\Omega$$

This is within the range of practical values and you can choose values from the E12 range of 68 kΩ or 82 kΩ. (The E12 range tells you which values of resistor are manufactured and easily available from suppliers.)

A test circuit can be set up on prototype board, as follows:



Prototype board layout for 555 astable circuit

With the values of *R*1, *R*2 and *C* shown, the LED should flash at around 10 Hz. How would you slow the rate of flashing to 1 Hz? Experiment to find a solution.

What happens if you replace *R*2 with an LDR or a thermistor? This gives an astable which changes frequency in response to light intensity, or with temperature.

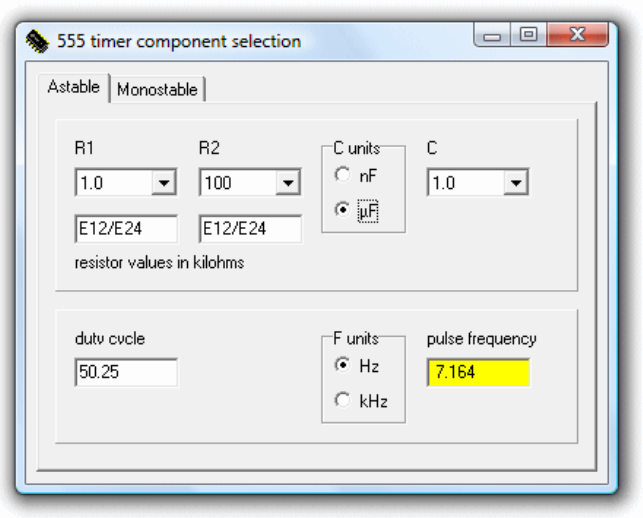
Clicking the button under the diagram moves you on to the next prototype board layout on this page. Clicking opens the drawing in a new window which you can maximise to fill the screen: there's no excuse for putting a wire link in the wrong place! Clicking opens a small window showing the pin layout for the 555, so that you can remind yourself which pin is which. The pins window remains open and can be brought to the front from the task bar at the bottom of the screen, unless you choose to close it.

Astables turn up in all sorts of places, as you can see from the Halloween toy skull with flashing red LED eyes.

3. Astable component selection

With a little practice, it is quite easy to choose appropriate values for a 555 timer astable. To make things even easier, you might like to download the DOCTRONICS 555 timer component selection program.

The program works with all versions of *Windows*™ from *Windows 95*™ through to *Windows Vista*™ and looks like this:

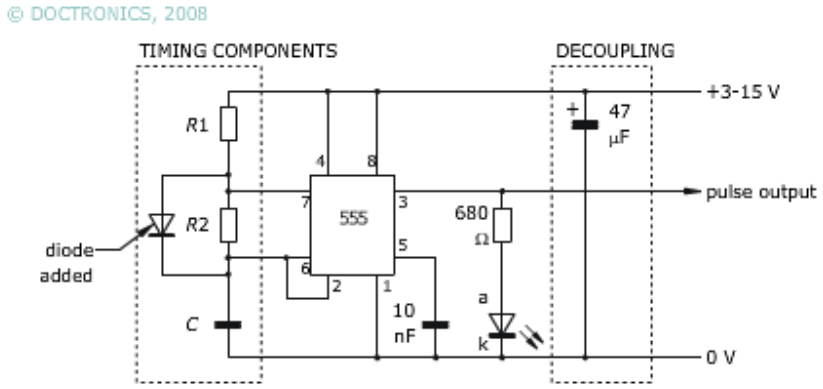


To download the program (~210K), click on its image. You can save the program to your own computer to use whenever you want.

4. More astables

4.1. Extended duty cycle astable

An extremely useful variation of the standard astable circuit involves adding a diode in parallel with *R*2:



Extended duty cycle astable

This simple addition has a dramatic effect on the behaviour of the circuit. The timing capacitor, *C*, is now filled *only* through *R*1 and emptied *only* through *R*2.

The design equation for the output pulse frequency is:

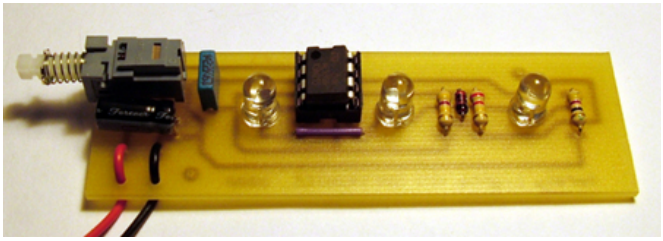
$$f = \frac{1.44}{(R1 + R2) \times C}$$

HIGH and LOW times are calculated from:

$$\text{HIGH time} = 0.69(R1 \times C) \qquad \text{LOW time} = 0.69(R2 \times C)$$

With this circuit, the duty cycle can be any value you want. If *R*1 > *R*2, the duty cycle will be greater than 50% (equivalent to a mark space ratio of more than 1.0). On the other hand, if *R*1 < *R*2, the duty cycle will be less than 50% (mark space ratio less than 1.0).

This is the version of the 555 astable is used in the DOCTRONICS safety lights project:



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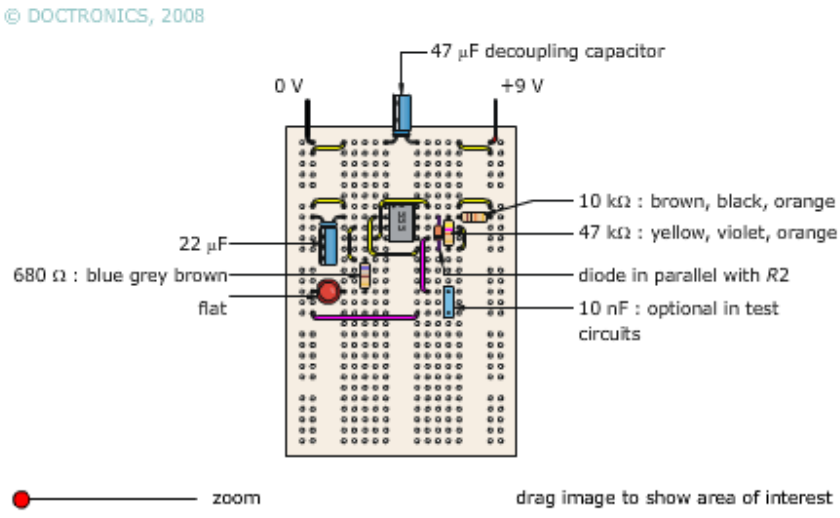
DOCTRONICS safety lights construction kit

You can see the extended duty cycle astable in action by building it on prototype board:

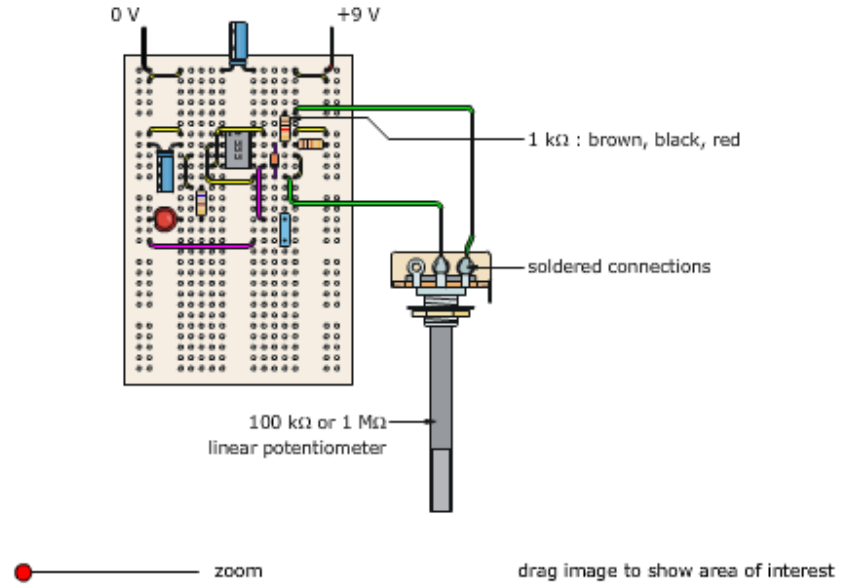


Extended duty cycle astable

The components used here are not the same as those in the test circuit for the normal version of the astable. *R*1=10 kΩ, *R*2=47 kΩ, and the timing capacitor *C*=22 µF.

With the diode in place, the HIGH time, when the LED is ON, should be around 0.69(0.01x22)=0.15 s (0.01 is 10 kΩ converted to MΩ). The LOW time should be visibly longer, 0.69(0.047x22)=0.71 s (0.047 is 47 kΩ converted to MΩ). What happens if you temporarily remove the diode from the circuit?

Replace the diode and then replace *R*2 with a 100 kΩ or a 1 MΩ potentiometer as indicated in the next prototype board layout:



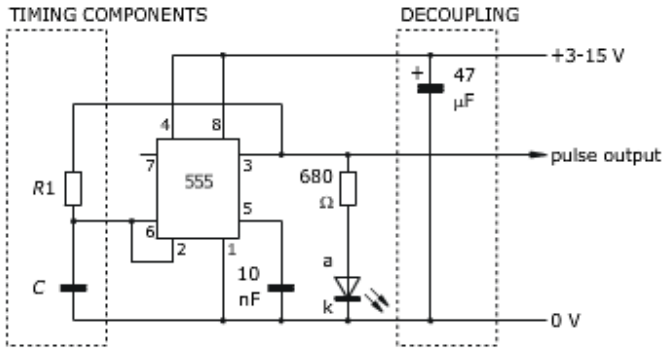
Adding a potentiometer

The 1 kΩ in series with the potentiometer, used here as a variable resistor, prevents you from adjusting *R*2 to zero. You need to solder single core wire to the potentiometer terminals: twisting the wire round the terminal doesn't make an effective connection.

As you adjust *R*2, the ON time of the LED remains constant, while the OFF time varies. Unlike the normal version of the 555 astable, the ON time can be short compared with the OFF time.

4.2 Minimum component astable

This is a cheap and cheerful astable using just one resistor and one capacitor as the timing components:



Minimum component astable

Note that there is no connection to pin 7 and that *R*1 is linked to the output, pin 3.

The design equation for the circuit is:

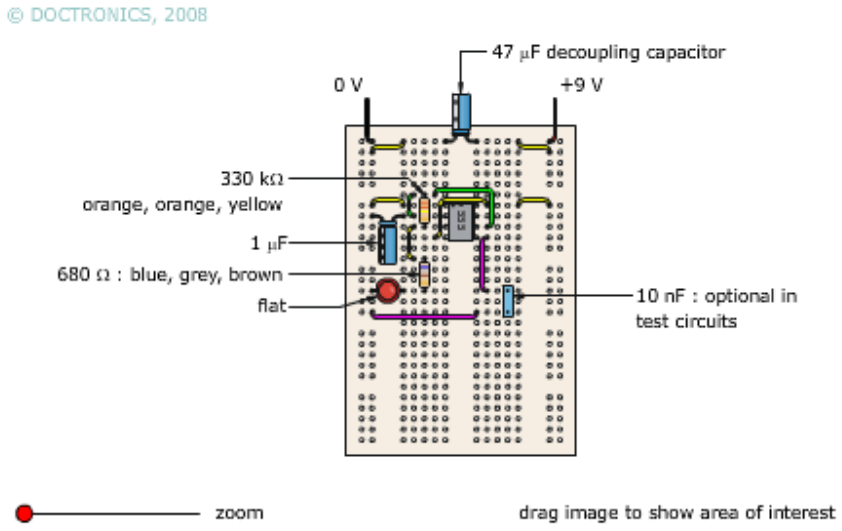
$$f = \frac{0.72}{R1 \times C}$$

The HIGH and LOW times are *supposed* to be equal, giving a duty cycle of 50% (equivalent to a mark space ratio of 1.0):

$$\text{HIGH time}=\text{LOW time} = 0.69(R1 \times C)$$

However, if you build this circuit, it is probable that the HIGH time will be longer than the LOW time. (This happens because the maximum voltage reached by the output pulses is less than the power supply voltage.) Things will get worse if the output current increases.

On protoytpe board, the circuit looks like this:



Minimum component astable

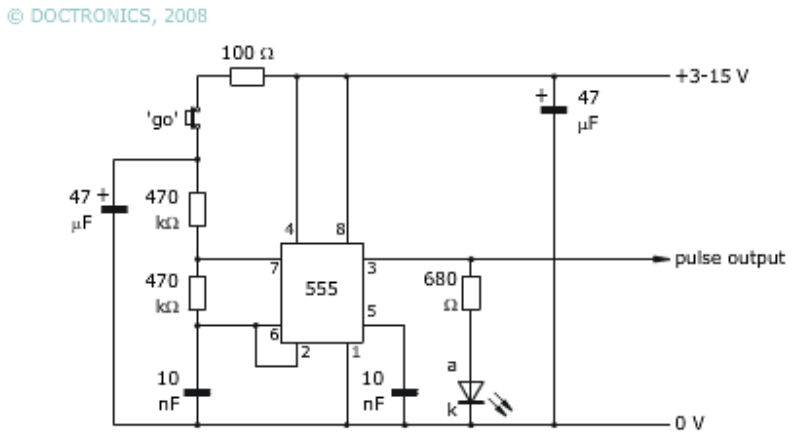
With the values shown, the frequency should be around 2.2 Hz.

If you need an astable circuit which can be adjusted to give an accurate frequency, this circuit is *not* the one to choose.

4.3 Diminishing frequency astable

The excitement and realism of electronic games, including roulette, can be increased using an astable circuit which is triggered to produce rapid pulses initially, but which then slows down and eventually stops altogether.

It is easy to modify the basic 555 astable circuit to produce this result:

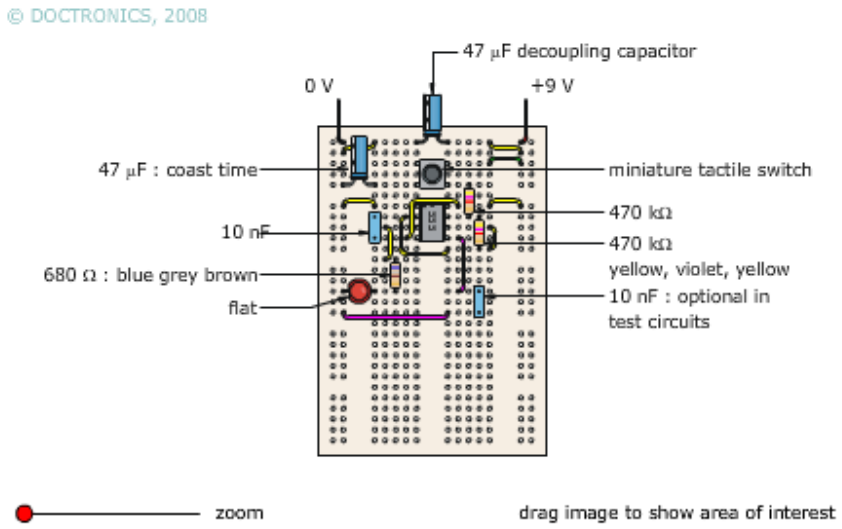


Diminishing frequency astable

When the 'go' button is pressed, the 47 µF capacitor in parallel with the timing network, *R*1, *R*2 and *C*, charges up very quickly through the 100 Ω resistor. When the button is released, the astable continues to oscillate but the charge stored slowly leaks away, with the result that it takes longer and longer to charge up the timing capacitor. To trigger the next pulse, the voltage across *C* must increase to two thirds

of the power supply voltage. After a while, the voltage across the 47 µF drops below this value and the pulses stop.

With the values shown, the initial frequency is about 100 Hz and the output pulses coast to a stop after around 40 seconds:



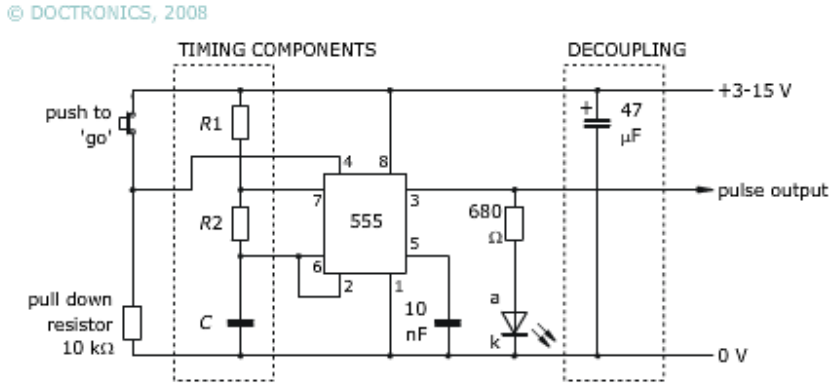
Diminishing frequency astable

The initial frequency can be calculated from the design equation for the basic 555 astable. To give a realistic coasting time, you should use large values for the resistors *R*1 and *R*2. The coasting time is determined by the 47 µF capacitor. Experiment with different values until you get the effect you want.

---

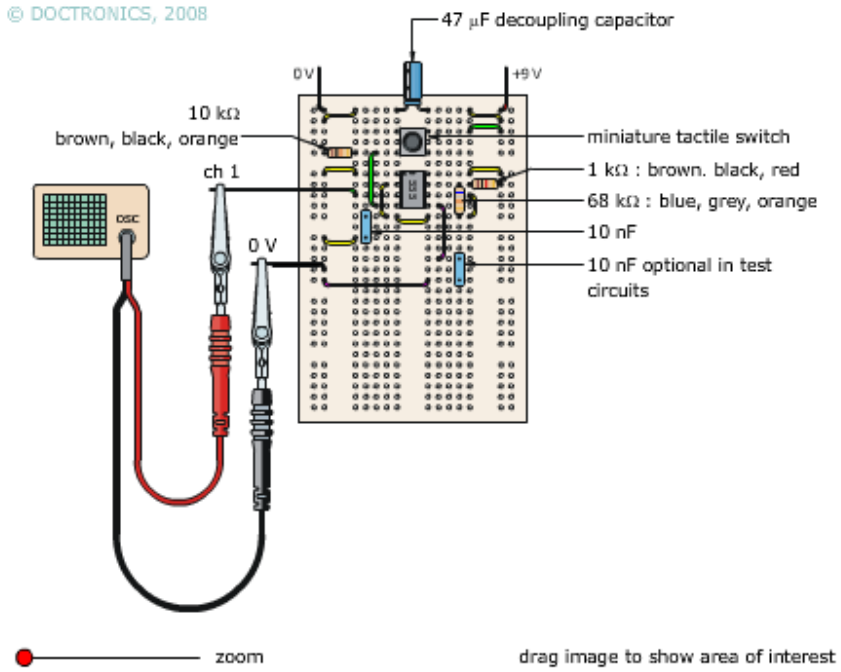
5. RESET input

If the RESET input, pin 4, is held HIGH, a 555 astable circuit functions as normal. However, if the RESET input is held LOW, output pulses are stopped. You can investigate this effect by connecting a switch/pull down resistor voltage divider to pin 4:



Investigating the RESET input

Here is the circuit on prototype board:



Investigating the RESET input

Use the design formula, or the DOCTRONICS component selector program to calculate the frequency of pulses you would expect to obtain with this circuit. Monitor the output pulses with an oscilloscope to check that your calculation is correct.

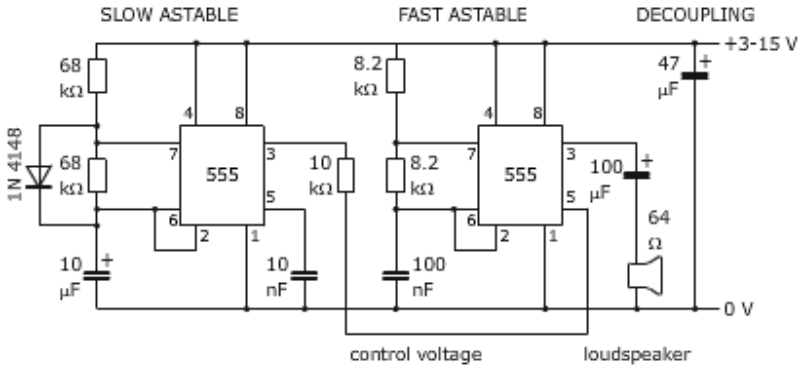
In an electronic die, provided the output pulses are fast enough, it is impossible to 'cheat' by holding down the button for a definite length of time. This is the circuit used in the DOCTRONICS electronic die construction kit:

Think about how you could use this circuit together with a bistable as part of a burglar alarm. Under normal conditions, the output of the bistable is LOW and the astable is stopped. If the alarm is triggered, the output of the bistable goes HIGH and the pulses start, sounding the alarm.

6. CONTROL VOLTAGE input

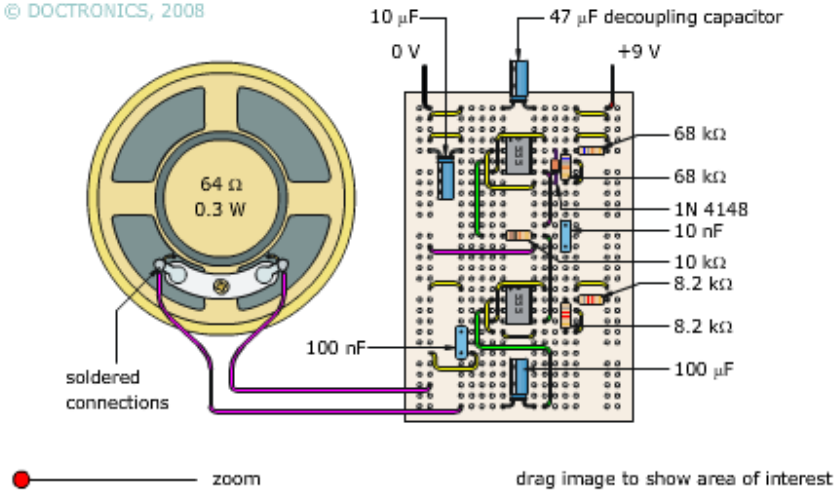
By applying a voltage to the CONTROL VOLTAGE input, pin 5, you can alter the timing characteristics of the device. In the astable mode, the control voltage can be varied from 1.7 V to the power supply voltage, producing an output frequency which can be higher or lower than the frequency set by the *R*1, *R*2, *C* timing network.

The CONTROL VOLTAGE input can be used to build an astable with a frequency modulated output. In the circuit below, one astable is used to control the frequency of a second, giving a 'police siren' sound effect:



UK police siren sound effect

Here is the prototype board layout:



UK police siren sound effect

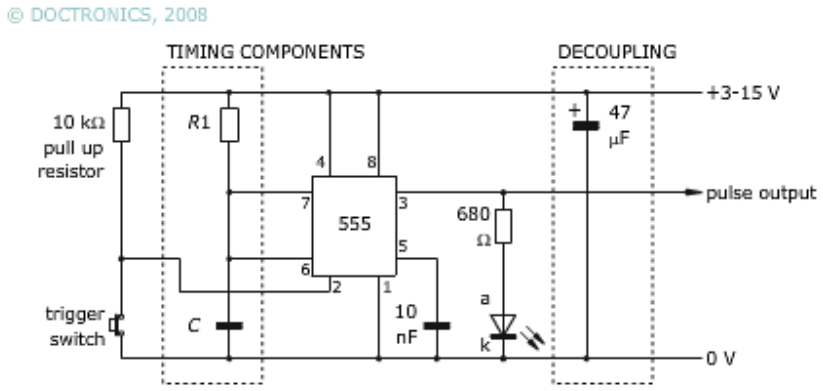
In most applications, the CONTROL VOLTAGE input is not used. It is usual to connect a 10 nF capacitor between pin 5 and 0 V to prevent interference. You don't need to do this in building a test circuit, although it is shown in the prototype board layouts, but this 'bypass' capacitor should be included in your final circuit.

7. Monostable circuits

A monostable, or one-shot, circuit produces a single pulse when triggered. The two questions about monostables you immediately need to ask are:

- How can the circuit be *triggered* to produce an output pulse?
- How is the duration, or *period*, of the output pulse determined?

The circuit used to make a 555 timer monostable is:



555 monostable circuit

As you can see, the trigger input is held HIGH by the 10 kΩ pull up resistor and is pulsed LOW when the trigger switch is pressed. The circuit is triggered by a falling edge, that is, by a sudden transition from HIGH to LOW.

The trigger pulse, produced by pressing the button, *must* be of shorter duration than the intended output pulse.

The period, t, of the output pulse can be calculated from the design equation:

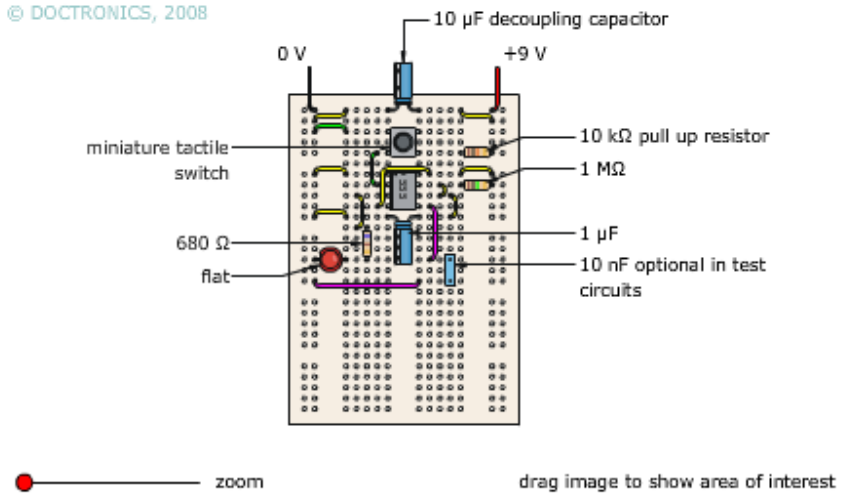
$$t = 1.1(R \times C)$$

Remember again about compatible measurement units:

resistance	*capacitance*	*period*
Ω	F	s
MΩ	µF	s
kΩ	µF	ms

With $R1$ = 1 MΩ and C = 1 µF, the output pulse will last for 1.1 s.

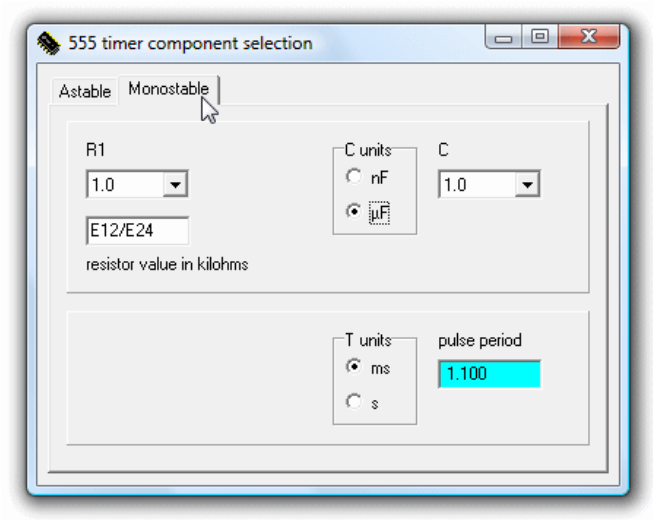
You can build a test version of the 555 monostable as follows:



555 monostable circuit

By clicking on the monostable tab, the 555 component selection program can be used

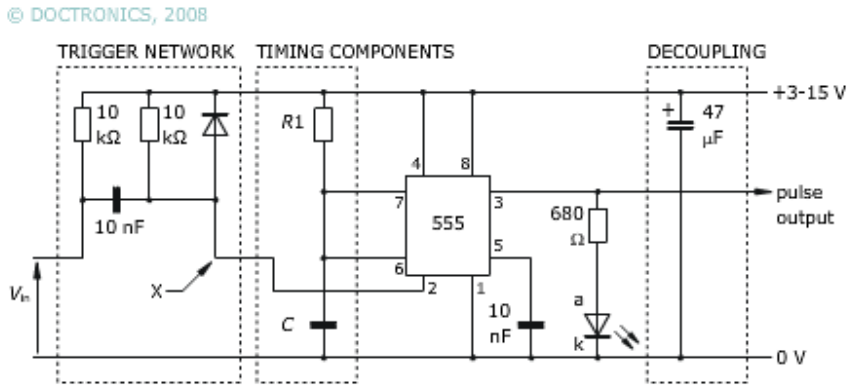
to investigate the effect of different *R*1 and *C* values:



To download the program (~210K), click on its image.

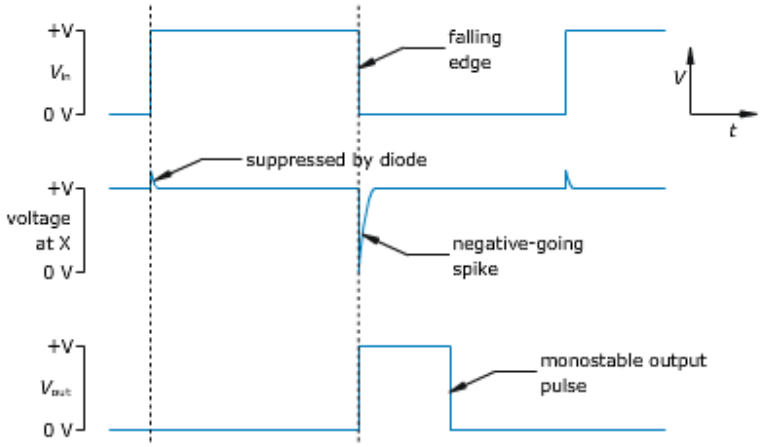
8. More about triggering

For a simple 555 monostable, the trigger pulse must be shorter than the output pulse. Sometimes you want to trigger the monostable from a longer pulse:



Adding a trigger network

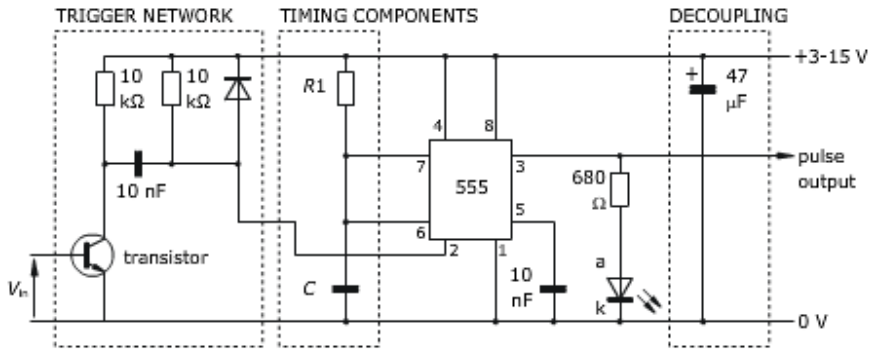
As you can see in the *V/t* graphs below, the voltage at X is normally held HIGH. A positive-going 'spike' would be generated on the rising edge of the V_{in} signal, but this is suppressed by the diode. On the other hand, the trigger network detects the falling edge at the end of each V_{in} pulse, producing a short negative-going spike which triggers the monostable:



V/t graphs for monostable with trigger network

The period of the monostable pulse is shorter than the period of the V_{in} pulses.

If you want to trigger the monostable from a rising edge, you need to add a transistor NOT gate to the trigger circuit:

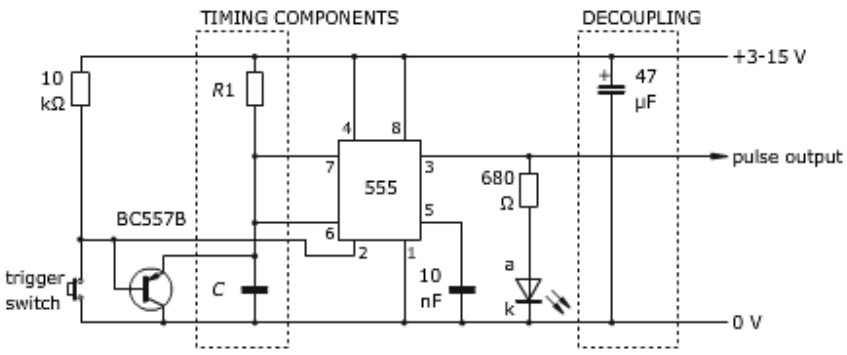


Triggering from a rising edge

If you build these circuits, it is interesting to investigate the action of the trigger network using an oscilloscope.

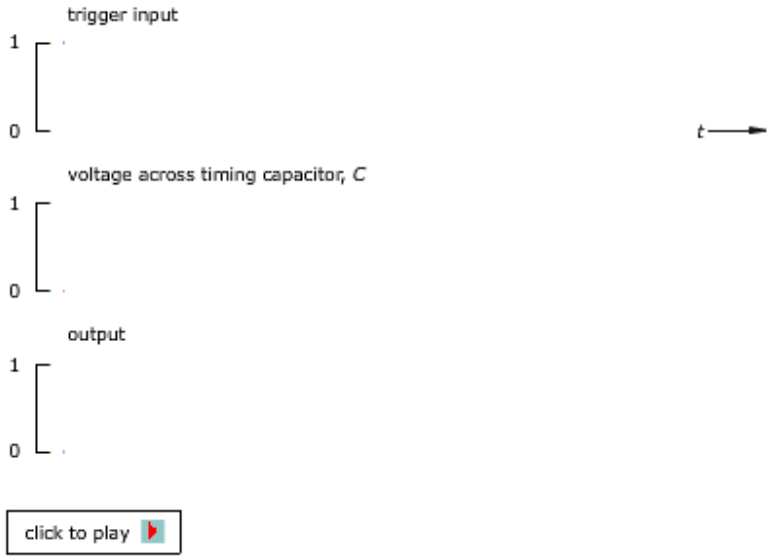
9. Retriggerable monostable

Another version of the monostable circuit allows you to initiate a new monstable pulse before any ongoing pulse has been completed:



Retriggerable monostable

As you can see, a PNP transistor, BC557B, has been added to the trigger circuit. To understand how the circuit works click 'play' in the animation:

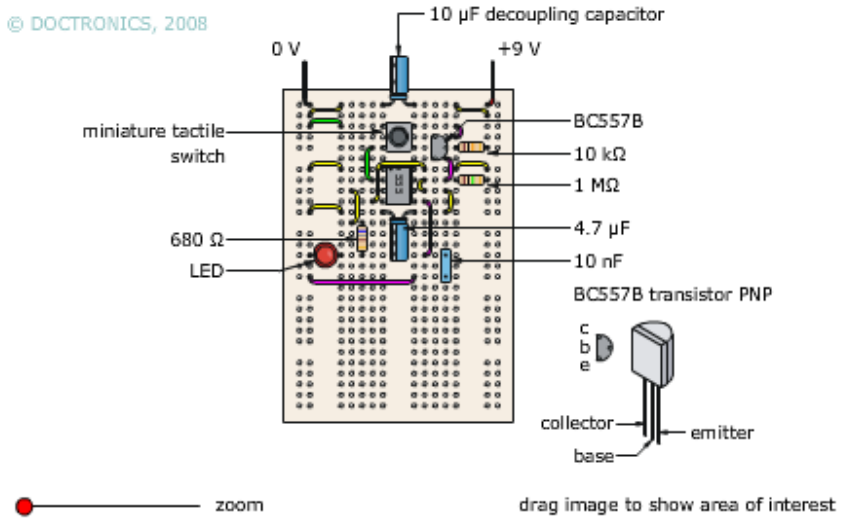


Waveforms for retriggerable monostable

The first trigger pulse results in a normal ouput pulse with a period determined by t=1.1*RC*. Note that the timing capacitor is fully discharged during the trigger pulse: the timing period starts when the trigger input goes HIGH.

The second trigger pulse is followed by a third and then a fourth before the normal output period has been completed. The additional trigger pulses discharge the timing capacitor, giving an extended output pulse.

To see this circuit in action, the prototype board layout for the standard 555 monostable can be modified, as follows:



Retriggerable monostable circuit

Operate the push switch. The normal output of the monostable should be around 5 s. When the LED switches OFF, press the push switch again and then press is once more after 2-3 s.

Provided you keep pressing the switch at intervals of less than 5 s, the output LED remains ON.

If the input voltage divider is replaced by a source of pulses, this circuit can be used

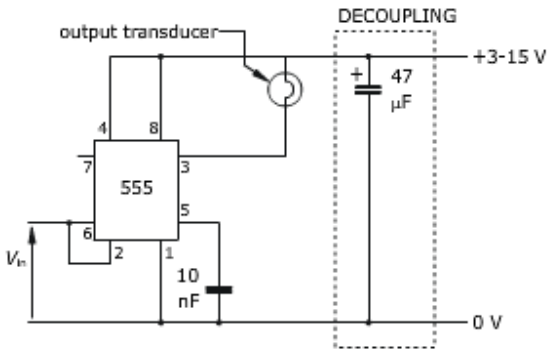
as a 'missing pulse' or 'low rate' detector. Any decrease in the frequency of the input pulses below the design level, will allow the monostable to complete its cycle, driving the output LOW.

10. 555 as a transducer driver

A transducer is a subsytem which converts energy from one form into another, where one of the forms is electrical. In an output transducer, for example, electrical energy can be converted into light, sound, or movement.

The output of a 555 timer can source or sink up to 200 mA of current. This means that output transducers including buzzers, filament lamps, loudspeakers and small motors can be connected directly to the output of the 555, pin 3.

You can use the 555 as a transducer driver, that is, as an electronic switch which turns the transducer ON or OFF:



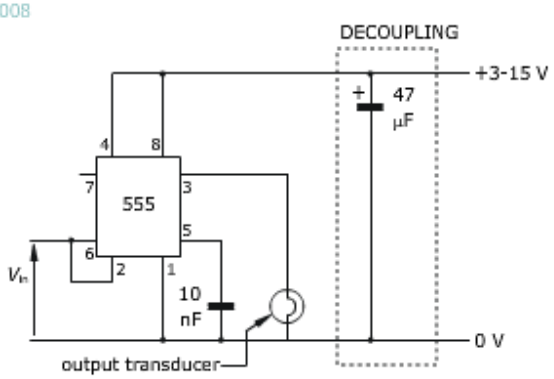
555 as a transducer driver

This circuit has an inverting Schmitt trigger action. The 'inverting' part of this description means that when V_{in} is LOW, the output is HIGH, and when V_{in} is HIGH, the output is LOW.

In a Schmitt trigger circuit there are two different switching thresholds. If V_{in} is slowly increased starting from 0 V, the output voltage snaps from HIGH to LOW when *V*in reaches a level equal to 2/3 of the power supply voltage. Once this level has been exceeded, decreasing *V*in does not affect the output until V_{in} drops below 1/3 of the power supply voltage. (If an input change in one direction produces a different result from a change in the opposite direction, the circuit is said to show hysteresis.)

If a filament lamp is connected between the positive power supply rail and the output, as shown above, current flows through the lamp when the output voltage is LOW. In other words, the lamp lights when the input voltage is HIGH.

If you connect the lamp between the output and 0 V, the circuit will still work, but the lamp will light when the input voltage is LOW:



555 as a transducer driver

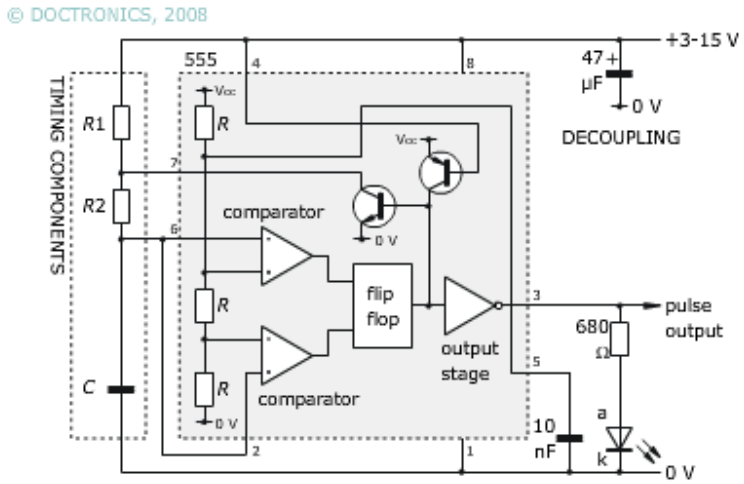
Note that, in both versions of the circuit pins 2 and 6 are joined together. The circuit can be simplified by omitting the 10 nF bypass capacitor, and will continue to work when the RESET input, pin 4 is left unconnected.

Some people are very fond of this circuit and use it whenever a transducer driver is required. However, with a HIGH/LOW digital input signal the same result can be achieved more obviously and at lower cost using a transistor switch circuit.

11. Inside the 555

You can use the 555 timer without knowing anything at all about its internal circuit. On the other hand, you might *like* to know something about what is going on inside.

The diagram below shows the 555 timer in astable mode with the internal circuit shown in block diagram form:



555 Internal block diagram

Inside the 555 you can see three resistors, labelled *R*. These resistors are equal in value and form a voltage divider, providing reference voltages at 1/3 and 2/3 of the power supply voltage, V_{CC}.

The reference voltages are connected to one input of each of two comparators, which in turn control the logic state of a bistable, or flip flop stage.

Pin 2 of the 555 is the trigger input. When the voltage connected to pin 2 is less than 1/3 of the power supply voltage, the output of the lower comparator forces the logic state of the flip flop to LOW. The output stage has an inverting action. In other words, when the output of the flip flop is LOW, the output of the 555 goes HIGH.

Now think about what happens when the power supply is first connected to the astable circuit. Initially, timing capacitor *C* is discharged. The voltage at pin 2 is 0 V and the output of the 555 is driven HIGH. *C* starts to charge through resistors *R*1 and *R*2. Note that *C* is also connected to pin 6, the threshold input of the 555.

When the voltage across *C* goes past 1/3 of the power supply voltage, the output of the lower comparator snaps a new level. This doesn't change the logic state of the flip flop: its output remains LOW.

The inputs to the second comparator are the voltage at pin 6, the threshold input, and 2/3 V_{CC} from the internal voltage divider.

When the voltage across *C* goes past 2/3 of the power supply voltage, the output of the second comparator snaps to a new level, the flip flop changes state, its output becomes HIGH and the output of the 555 goes from HIGH to LOW.

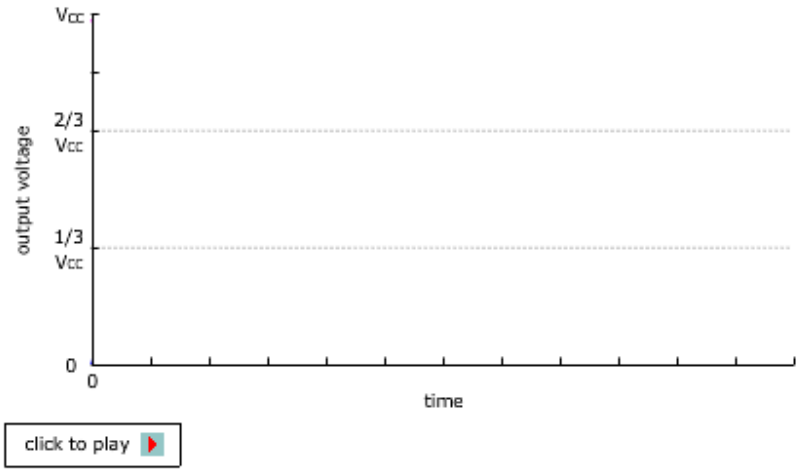
Inside the 555, the flip flop is connected to an NPN transistor, the collector of which is connected to pin 7, the discharge pin of the 555. When the output of the flip flop

goes HIGH, the transistor is switched ON, providing a low resistance path from the discharge pin to 0 V. The timing capacitor, *C*, starts to empty through *R*2 and the voltage across it decreases.

Note that the capacitor charges through *R*1 and *R*2, but discharges only through *R2.*

When the voltage across *C* decreases below 1/3 of the power supply voltage, the lower comparator snaps to a new level, the flip flop changes state and the output of the 555 goes HIGH once again.

The graph below shows how the voltage across the timing capacitor, V_C , changes with the output voltage of the 555, V_{out}:



555 astable voltages

The initial ouptut pulse is longer than subsequent pulses because *C* is completely discharged when the power supply is first connected. Subsequent HIGH and low times correspond to half-charge/discharge times, either from 1/3 to 2/3 of the power supply voltage, or from 2/3 to 1/3 of the power supply voltage.

The HIGH time is given by:

$$\text{HIGH time} = 0.69(R1 + R2) \times C$$

Remember, *C* charges through both *R*1 and *R*2.

The LOW time is given by:

$$\text{LOW time} = 0.69R2 \times C$$

C discharges only through *R*2.

The period, *t*, of the 555 astable is given by:

$$t = 0.69(R1 + R2) \times C + 0.69R2 \times C = 0.69(R1 + 2R2) \times C$$

The frequency, *f*, is given by:

$$f = \frac{1}{t} = \frac{1}{0.69(R1 + 2R2) \times C} = \frac{1.44}{(R1 + 2R2) \times C}$$

Try 1÷0.69 on your calculator to confirm that it does equal 1.44.

The design formula for the 555 astable follows from the behaviour of *RC* networks and from the two switching thresholds of the voltage divider inside the device.

In a 555 monostable, only the upper threshold is used to determine the period, so the formula corresponds to a 2/3 charge time:

$$t = 1.1(R \times C)$$

You can find further details about the internal circuit of the 555 in the data sheets provided in the next section.

---

12. Links

10. 1 Data sheets

A great little book for just £4.99...

The links below allow you to download documents in *Adobe Acrobat* ©, PDF, format. In the unlikely event that you don't already have *Acrobat Reader*, you can download the latest version direct from *Adobe*:

555 data sheet *(Phillips Semiconductors, 1994)*

555 application note (*Philips Semiconductors AN 170, 1988*)

10. 2 Internet resources

555 Timer Tutorial (Tony van Roon, University of Guelph, Canada)

555 timer IC (from *Wikipedia*, the free encyclopaedia)

Doctronics Bookshelf

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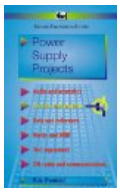

Power Supply Projects (BP)
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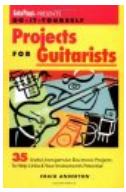

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ΕΡΓΑΣΤΗΡΙΟΥ
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National Semiconductor

August 2000

LF411
Low Offset, Low Drift JFET Input Operational Amplifier

General Description

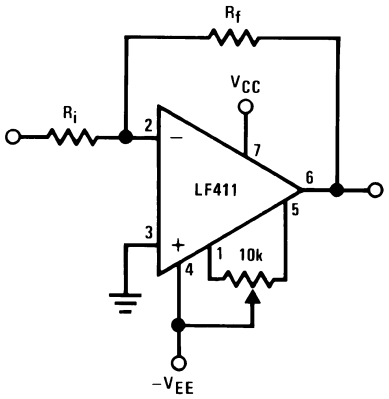
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage: 0.5 mV(max)
- Input offset voltage drift: 10 µV/°C(max)
- Low input bias current: 50 pA
- Low input noise current: 0.01 pA/√Hz
- Wide gain bandwidth: 3 MHz(min)
- High slew rate: 10V/µs(min)
- Low supply current: 1.8 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion: ≤0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 µs

Typical Connection



00565501

Ordering Information

LF411XYZ

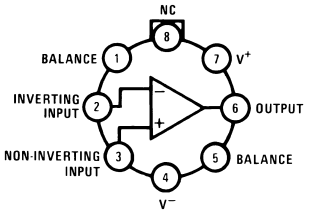
X indicates electrical grade

Y indicates temperature range
- "M" for military
- "C" for commercial

Z indicates package type
- "H" or "N"

Connection Diagrams

Metal Can Package



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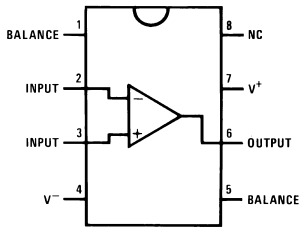
Note: Pin 4 connected to case.

Top View
Order Number LF411ACH
or LF411MH/883 (Note 11)
See NS Package Number H08A

Dual-In-Line Package



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Top View
Order Number LF411ACN, LF411CN
See NS Package Number N08E

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LF411A	LF411
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 2)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	H Package	N Package
Power Dissipation (Notes 3, 10)	670 mW	670 mW

	H Package	N Package
$T_j$max	150˚C	115˚C
θ_jA	162˚C/W (Still Air) 65˚C/W (400 LF/min Air Flow)	120˚C/W
θ_jC	20˚C/W	
Operating Temp. Range	(Note 4)	(Note 4)
Storage Temp. Range	−65˚C≤T_A≤150˚C	−65˚C≤T_A≤150˚C
Lead Temp. (Soldering, 10 sec.)	260˚C	260˚C
ESD Tolerance	Rating to be determined.	

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF411A			LF411			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10 kΩ, T_A=25˚C			0.3	0.5		0.8	2.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ (Note 6)			7	10		7	20 (Note 6)	µV/˚C
I_{OS}	Input Offset Current	V_S=±15V (Notes 5, 7)	T_j=25˚C		25	100		25	100	pA
			T_j=70˚C			2			2	nA
			T_j=125˚C			25			25	nA
I_B	Input Bias Current	V_S=±15V (Notes 5, 7)	T_j=25˚C		50	200		50	200	pA
			T_j=70˚C			4			4	nA
			T_j=125˚C			50			50	nA
R_{IN}	Input Resistance	T_j=25˚C			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, V_O=±10V, R_L=2k, T_A=25˚C		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	R_S≤10k		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)		80	100		70	100		dB
I_S	Supply Current				1.8	2.8		1.8	3.4	mA

AC Electrical Characteristic (Note 5)

Symbol	Parameter	Conditions	LF411A			LF411			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	V_S=±15V, T_A=25˚C	10	15		8	15		V/µs
GBW	Gain-Bandwidth Product	V_S=±15V, T_A=25˚C	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25˚C, R_S=100Ω, f=1 kHz		25			25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_A=25˚C, f=1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

AC Electrical Characteristic (Note 5) (Continued)

Symbol	Parameter	Conditions	LF411A			LF411			Units
			Min	Typ	Max	Min	Typ	Max	
THD	Total Harmonic Distortion	A_V=+10, R_L=10k, V_O=20 Vp-p, BW=20 Hz–20 kHz		<0.02			<0.02		%

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of $\theta_j A$.

Note 4: These devices are available in both the commercial temperature range $0^\circ C \le T_A \le 70^\circ C$ and the military temperature range $-55^\circ C \le T_A \le 125^\circ C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 5: Unless otherwise specified, the specifications apply over the full temperature range and for V_S=±20V for the LF411A and for V_S=±15V for the LF411. V_{OS}, I_B, and I_{OS} are measured at V_{CM}=0.

Note 6: The LF411A is 100% tested to this specification. The LF411 is sample tested to insure at least 90% of the units meet this specification.

Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

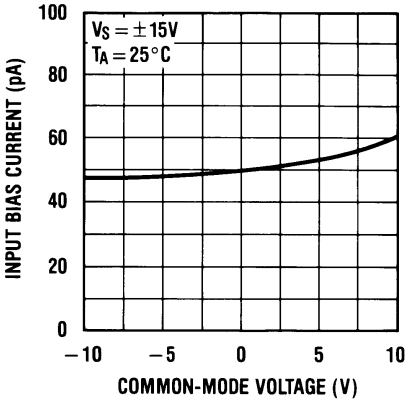
Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from ±15V to ±5V for the LF411 and from ±20V to ±5V for the LF411A.

Note 9: RETS 411X for LF411MH and LF411MJ military specifications.

Note 10: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

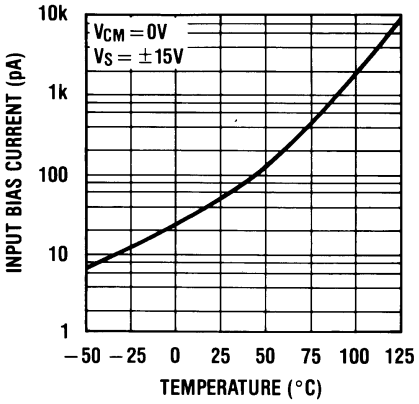
Typical Performance Characteristics

Input Bias Current



00565511

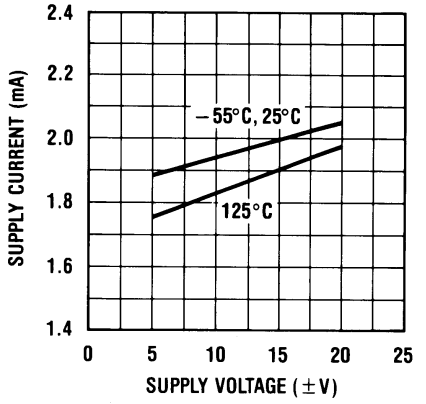
Input Bias Current



00565512

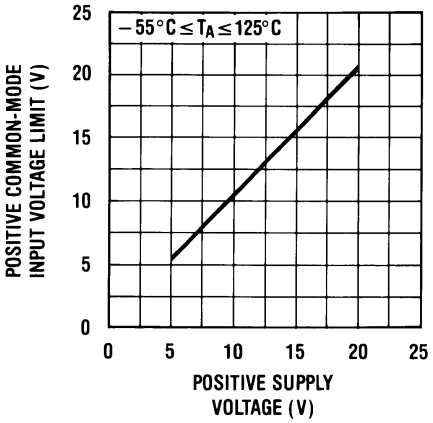
Typical Performance Characteristics (Continued)

Supply Current



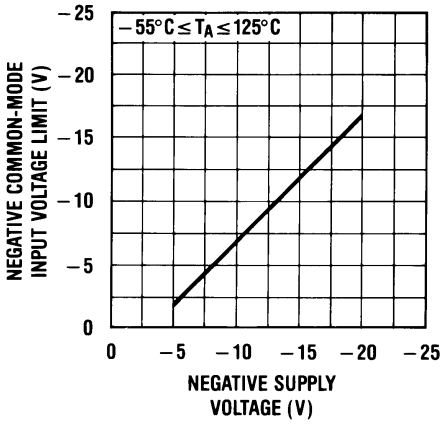
00565513

Positive Common-Mode Input Voltage Limit



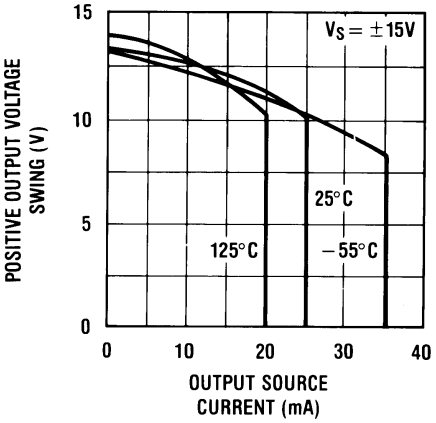
00565514

Negative Common-Mode Input Voltage Limit



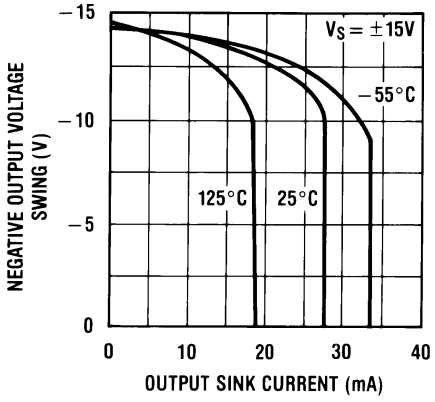
00565515

Positive Current Limit



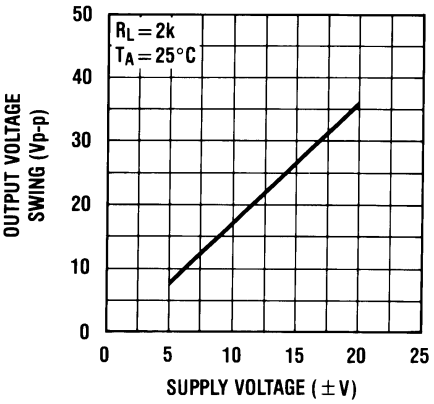
00565516

Negative Current Limit



00565517

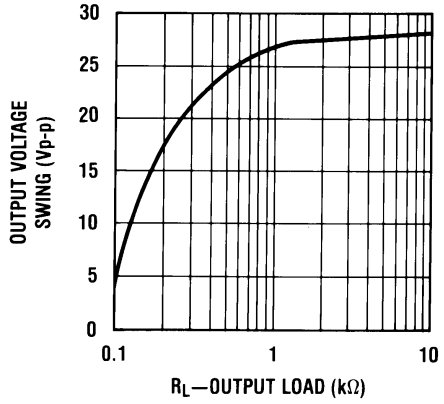
Output Voltage Swing



00565518

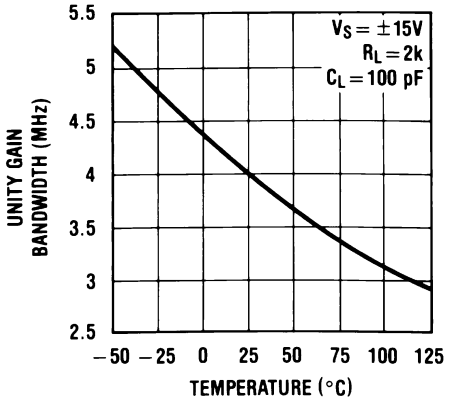
Typical Performance Characteristics (Continued)

Output Voltage Swing



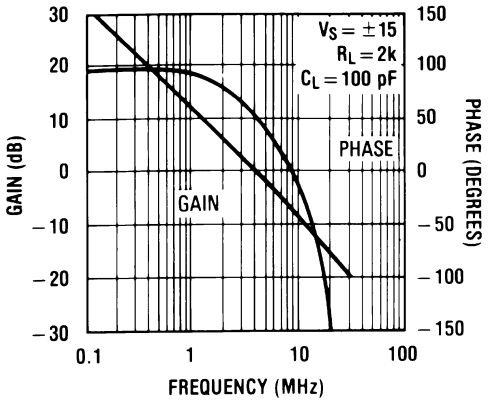
00565519

Gain Bandwidth



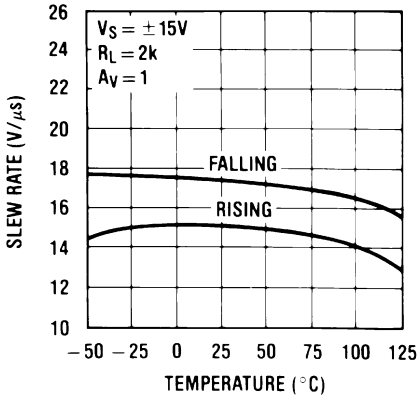
00565520

Bode Plot



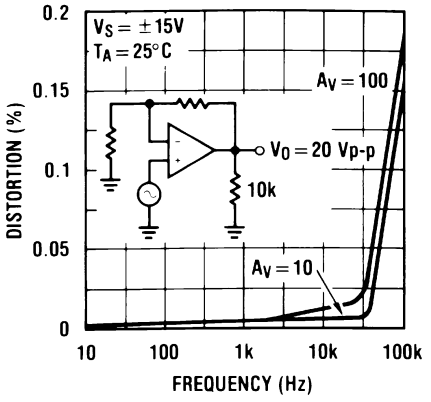
00565521

Slew Rate



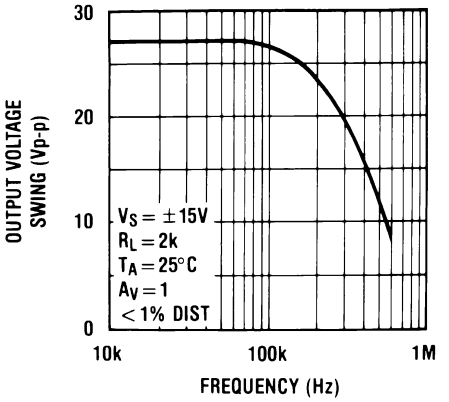
00565522

Distortion vs Frequency



00565523

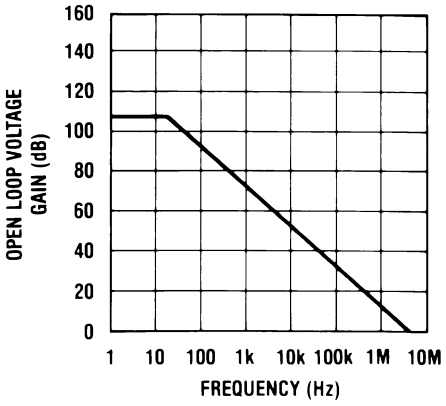
Undistorted Output Voltage Swing



00565524

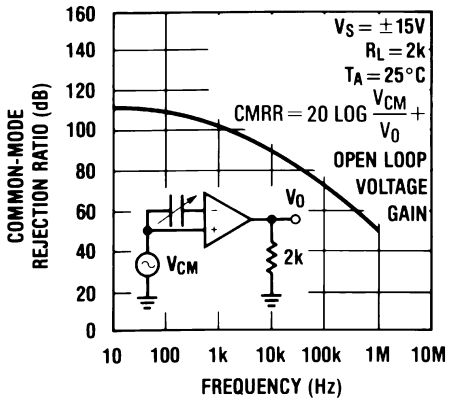
Typical Performance Characteristics (Continued)

Open Loop Frequency Response



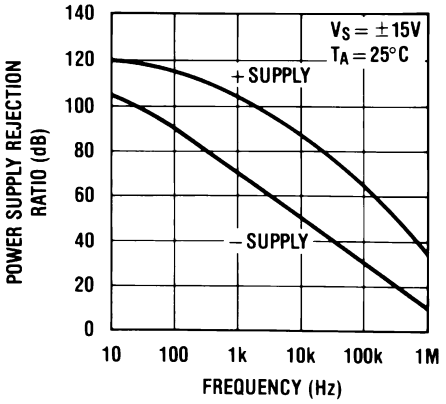
00565525

Common-Mode Rejection Ratio



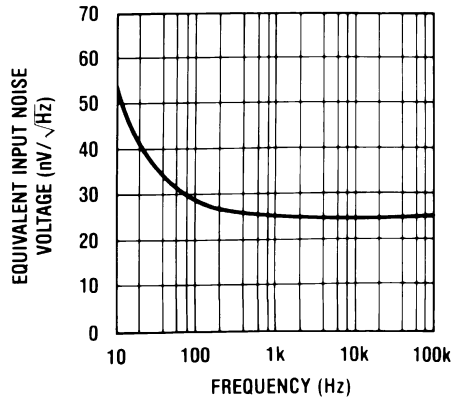
00565526

Power Supply Rejection Ratio



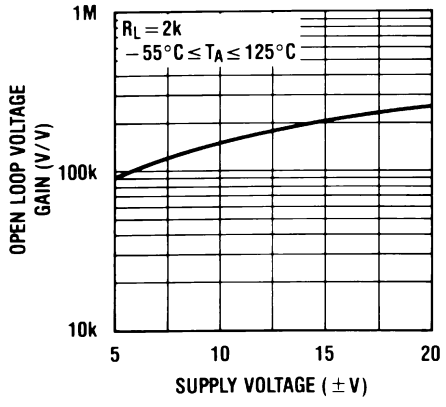
00565527

Equivalent Input Noise Voltage



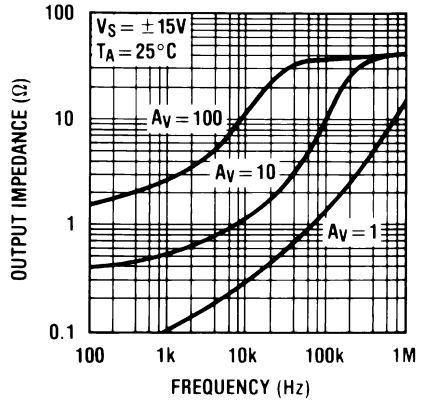
00565528

Open Loop Voltage Gain



00565529

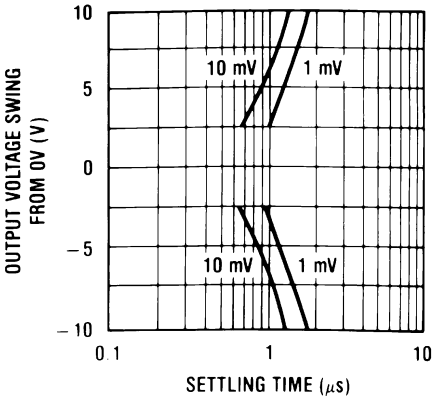
Output Impedance



00565530

Typical Performance Characteristics (Continued)

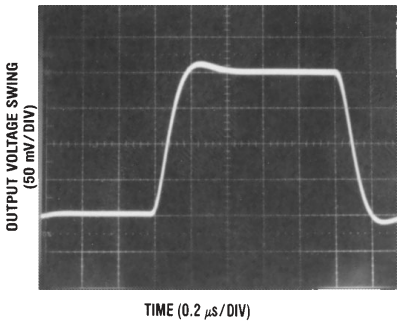
Inverter Settling Time



00565531

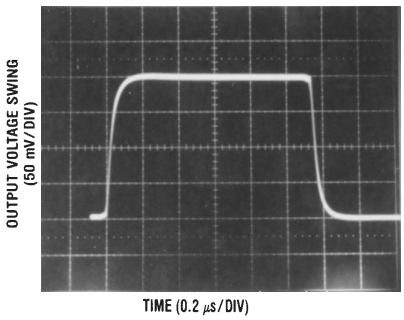
Pulse Response R_L=2 kΩ, C_L10 pF

Small Signal Inverting



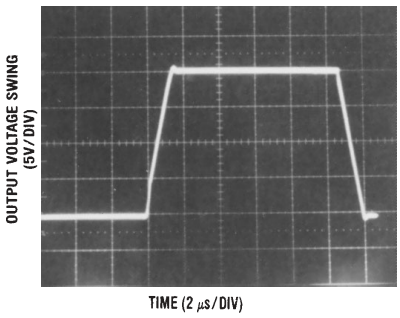
00565539

Small Signal Non-Inverting



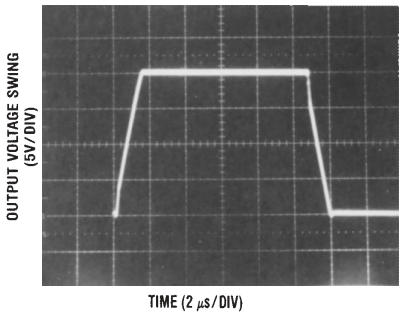
00565540

Large Signal Inverting



00565541

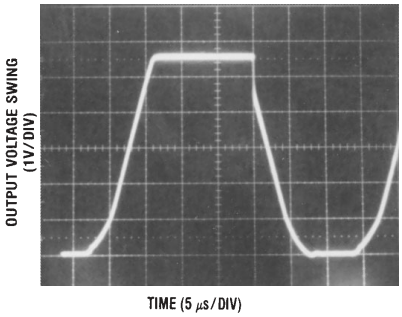
Large Signal Non-Inverting



00565542

Pulse Response R_L=2 kΩ, C_L10 pF (Continued)

Current Limit (R_L=100Ω)



00565543

Application Hints

The LF411 series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

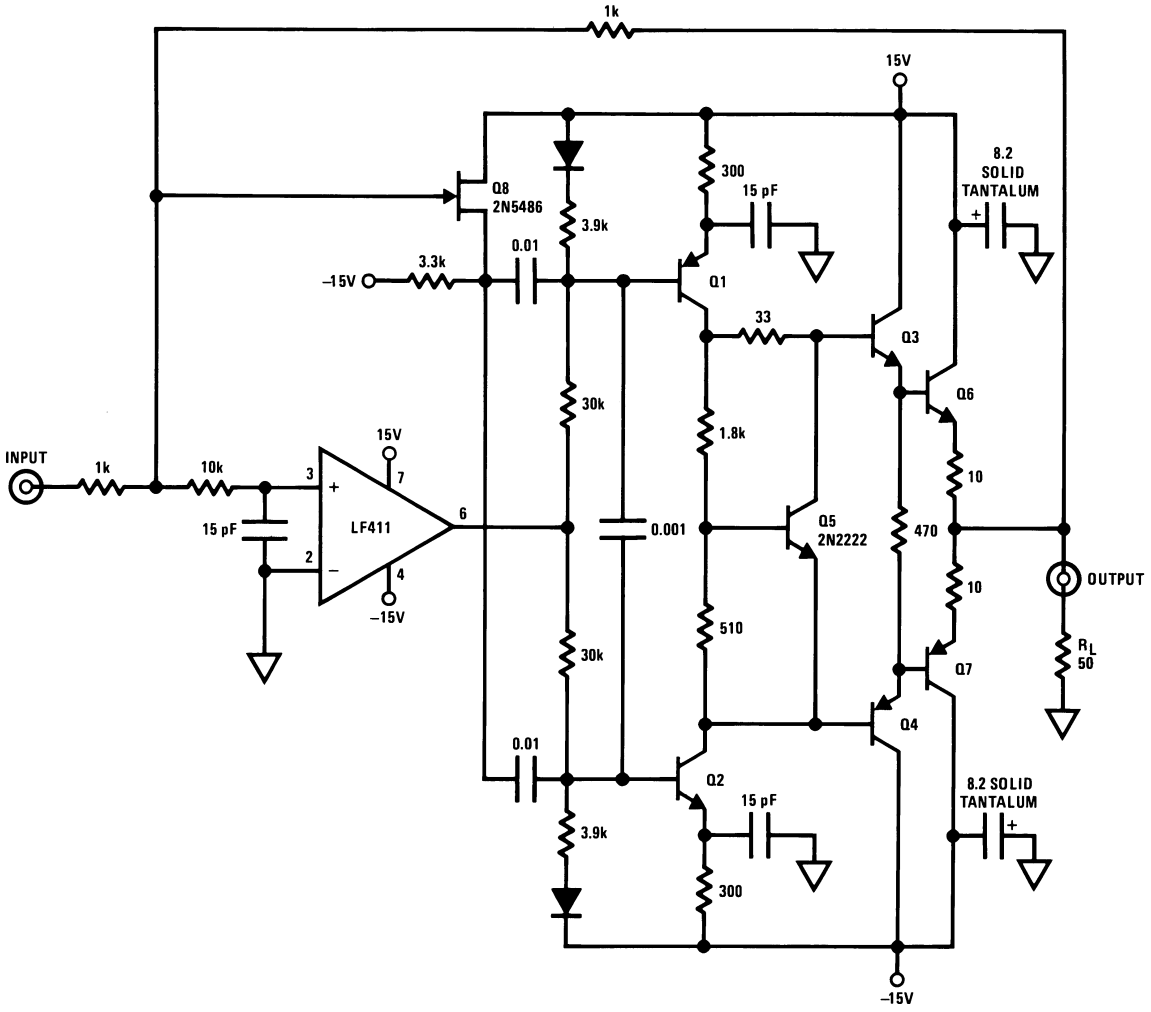
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

High Speed Current Booster



00565509

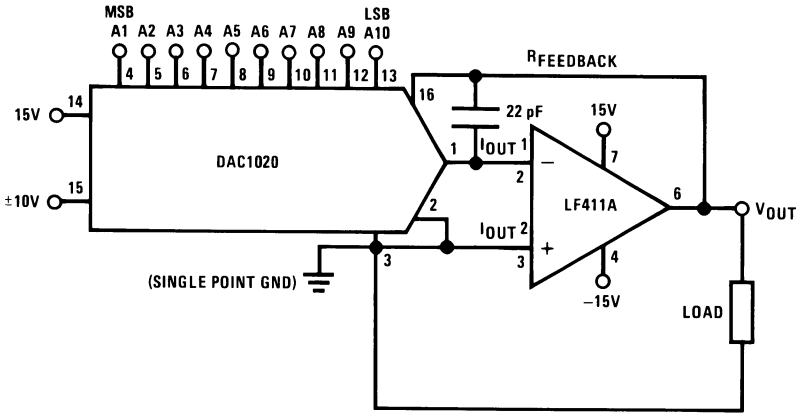
PNP=2N2905

NPN=2N2219 unless noted

TO-5 heat sinks for Q6-Q7

Typical Applications (Continued)

10-Bit Linear DAC with No V_{OS} Adjust



00565532

$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

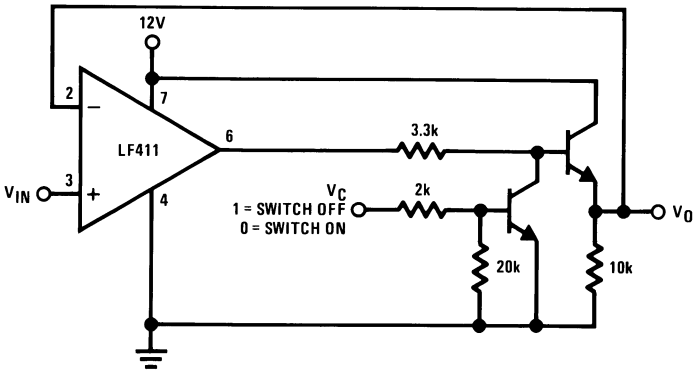
$$-10V \le V_{REF} \le 10V$$

$$0 \le V_{OUT} \le -\frac{1023}{1024} V_{REF}$$

where A_N=1 if the A_N digital input is high

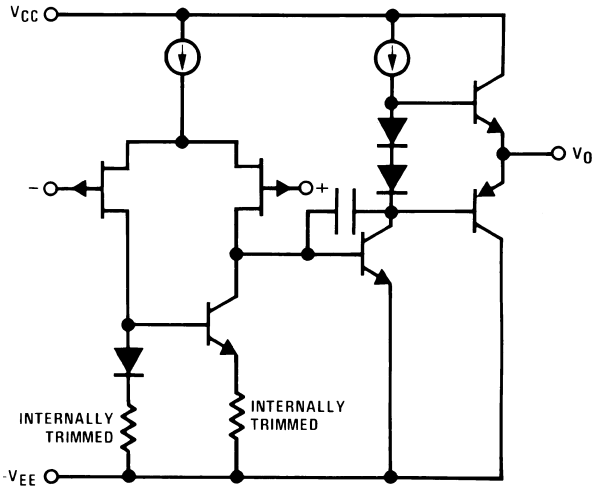
A_N=0 if the A_N digital input is low

Single Supply Analog Switch with Buffered Output



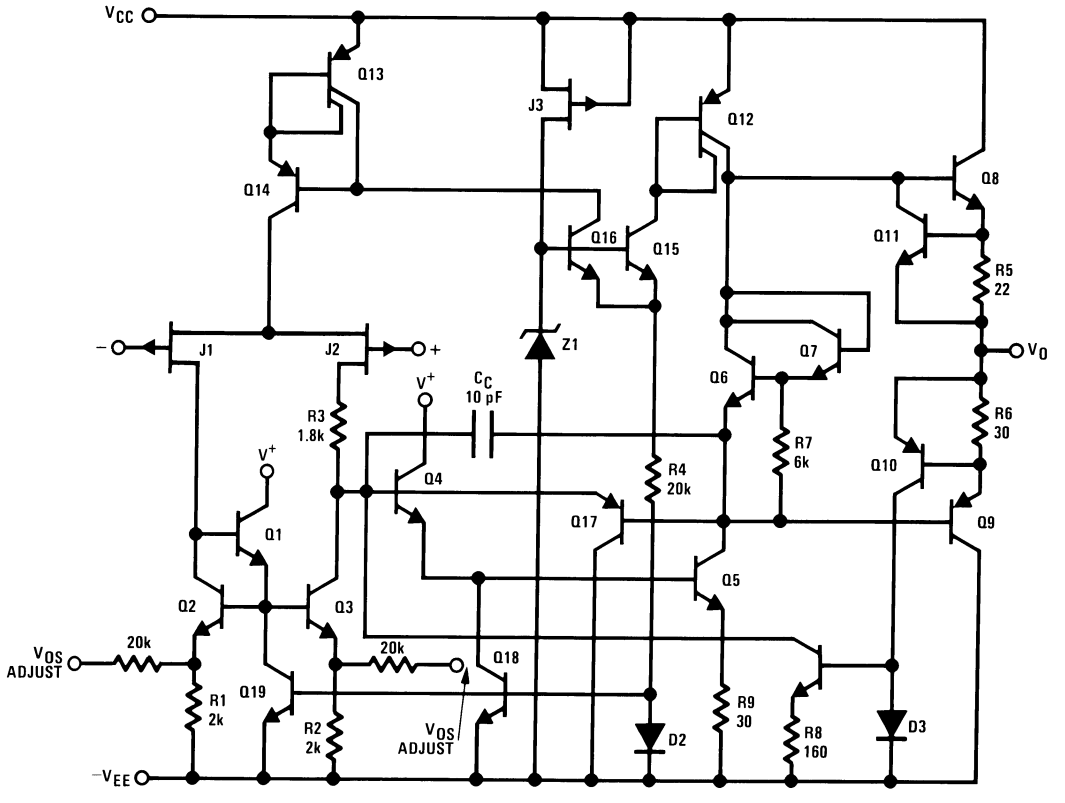
00565533

Simplified Schematic

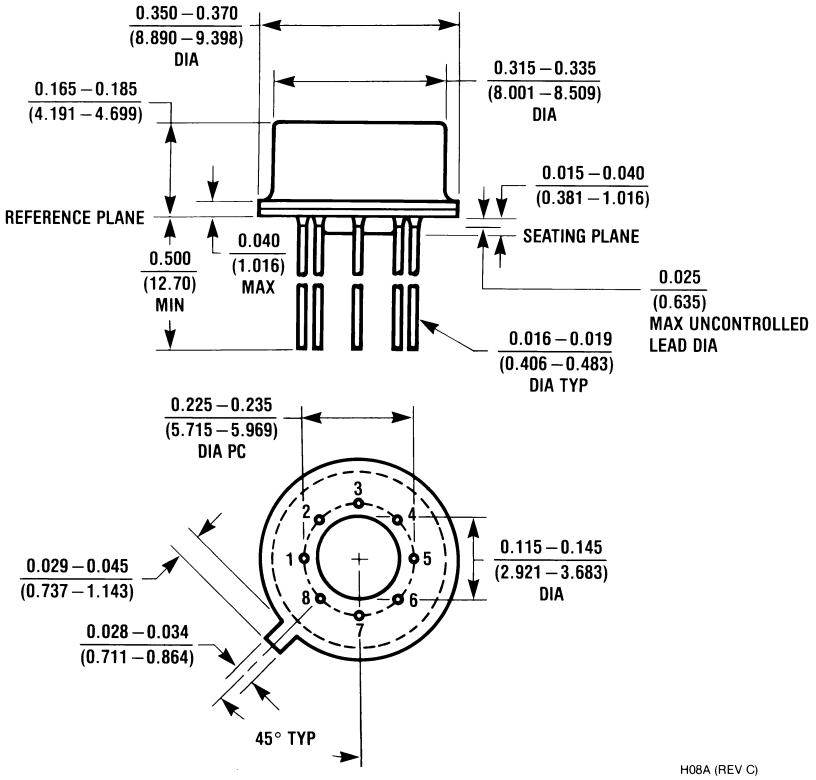


Note 11: Available per JM38510/11904

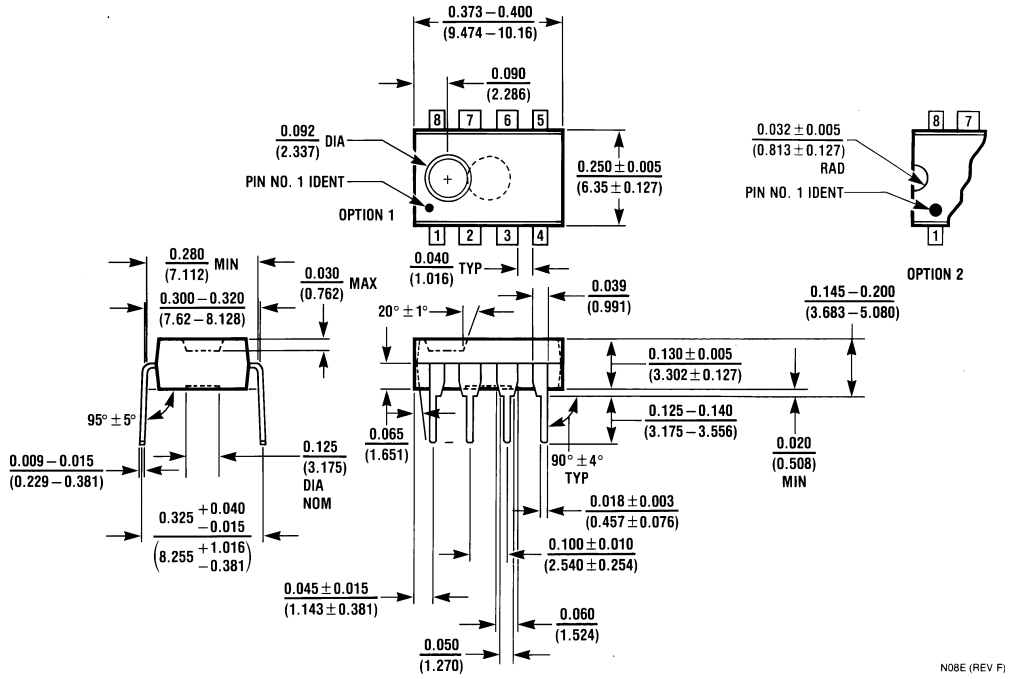
Detailed Schematic



Physical Dimensions inches (millimeters) unless otherwise noted



Metal Can Package (H)
Order Number LF411MH/883 or LF411ACH
NS Package Number H08A



Molded Dual-In-Line Package (N)
Order Number LF411ACN or LF411CN
NS Package Number N08E

Notes

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

August 2000

LM741
Operational Amplifier

General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

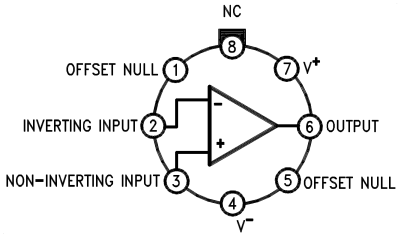
The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0˚C to +70˚C temperature range, instead of −55˚C to +125˚C.

Features

Connection Diagrams

Metal Can Package

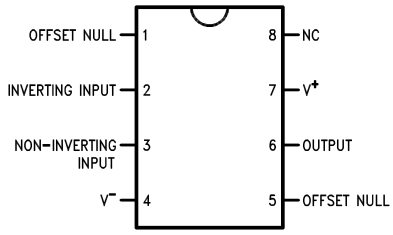


00934102

Note 1: LM741H is available per JM38510/10101

Order Number LM741H, LM741H/883 (Note 1)**, LM741AH/883 or LM741CH**
See NS Package Number H08C

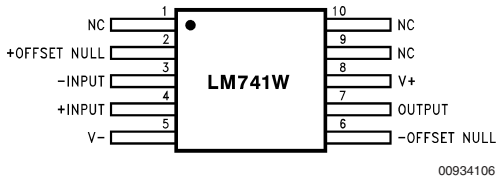
Dual-In-Line or S.O. Package



00934103

Order Number LM741J, LM741J/883, LM741CN
See NS Package Number J08A, M08A or N08E

Ceramic Flatpak

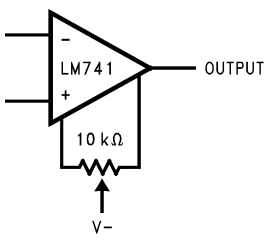


00934106

Order Number LM741W/883
See NS Package Number W10A

Typical Application

Offset Nulling Circuit



00934107

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 7)

	LM741A	LM741	LM741C
Supply Voltage	±22V	±22V	±18V
Power Dissipation (Note 3)	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V
Input Voltage (Note 4)	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Operating Temperature Range	−55˚C to +125˚C	−55˚C to +125˚C	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C	−65˚C to +150˚C	−65˚C to +150˚C
Junction Temperature	150˚C	150˚C	100˚C
Soldering Information			
N-Package (10 seconds)	260˚C	260˚C	260˚C
J- or H-Package (10 seconds)	300˚C	300˚C	300˚C
M-Package			
Vapor Phase (60 seconds)	215˚C	215˚C	215˚C
Infrared (15 seconds)	215˚C	215˚C	215˚C
See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.			
ESD Tolerance (Note 8)	400V	400V	400V

Electrical Characteristics (Note 5)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25˚C$										
	$R_S \le 10\ k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \le 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 50\Omega$			4.0							mV
	$R_S \le 10\ k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							µV/˚C
Input Offset Voltage Adjustment Range	$T_A = 25˚C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25˚C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/˚C
Input Bias Current	$T_A = 25˚C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	$T_A = 25˚C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25˚C$							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V

Electrical Characteristics (Note 5) (Continued)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$T_A = 25^\circ C$, $R_L \geq 2\ k\Omega$										
	$V_S = \pm 20V$, $V_O = \pm 15V$	50									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				50	200		20	200		V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
	$R_L \geq 2\ k\Omega$,										
	$V_S = \pm 20V$, $V_O = \pm 15V$	32									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				25			15			V/mV
	$V_S = \pm 5V$, $V_O = \pm 2V$	10									V/mV
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10\ k\Omega$	±16									V
	$R_L \geq 2\ k\Omega$	±15									V
	$V_S = \pm 15V$										
	$R_L \geq 10\ k\Omega$				±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$				±10	±13		±10	±13		V
Output Short Circuit	$T_A = 25^\circ C$	10	25	35		25			25		mA
Current	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Common-Mode	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50\Omega$, $V_{CM} = \pm 12V$	80	95								dB
Supply Voltage Rejection	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
Ratio	$V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \leq 50\Omega$	86	96								dB
	$R_S \leq 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25^\circ C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		µs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 6)	$T_A = 25^\circ C$	0.437	1.5								MHz
Slew Rate	$T_A = 25^\circ C$, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current	$T_A = 25^\circ C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25^\circ C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 2: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Electrical Characteristics (Note 5) (Continued)

Note 3: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100˚C/W	100˚C/W	170˚C/W	195˚C/W
θ_{jC} (Junction to Case)	N/A	N/A	25˚C/W	N/A

Note 4: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

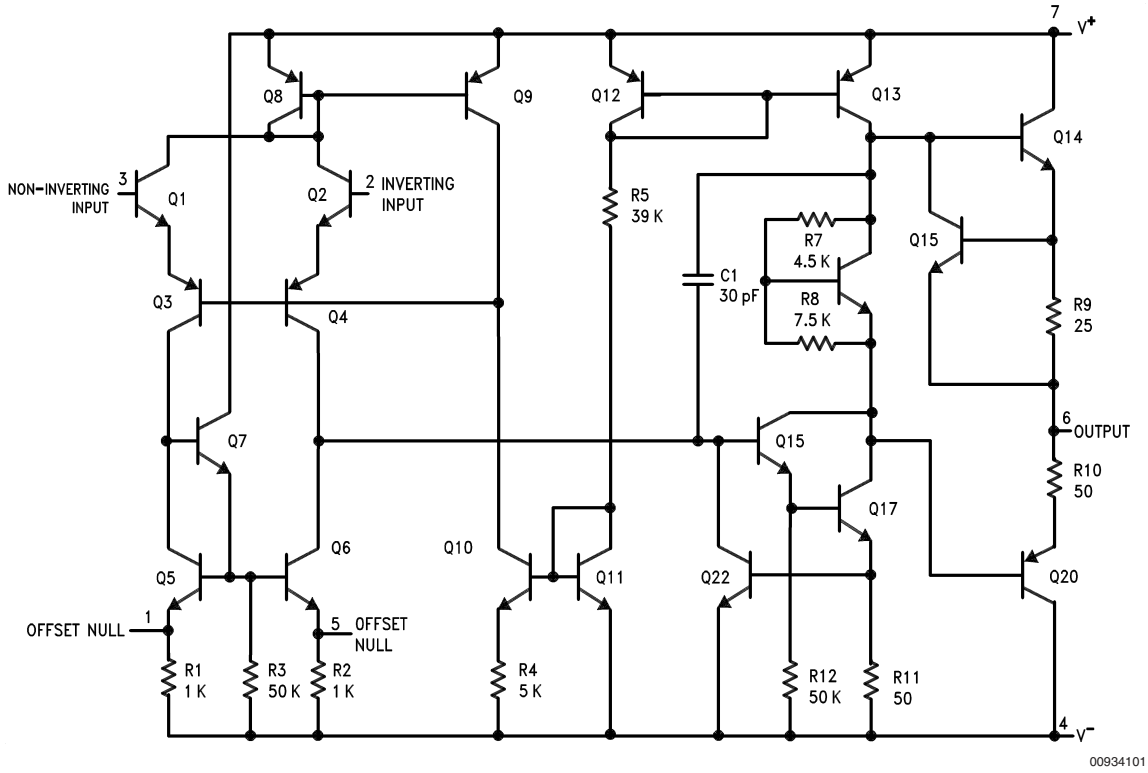
Note 5: Unless otherwise specified, these specifications apply for V_S = ±15V, −55˚C ≤ T_A ≤ +125˚C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0˚C ≤ T_A ≤ +70˚C.

Note 6: Calculated value from: BW (MHz) = 0.35/Rise Time(μs).

Note 7: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

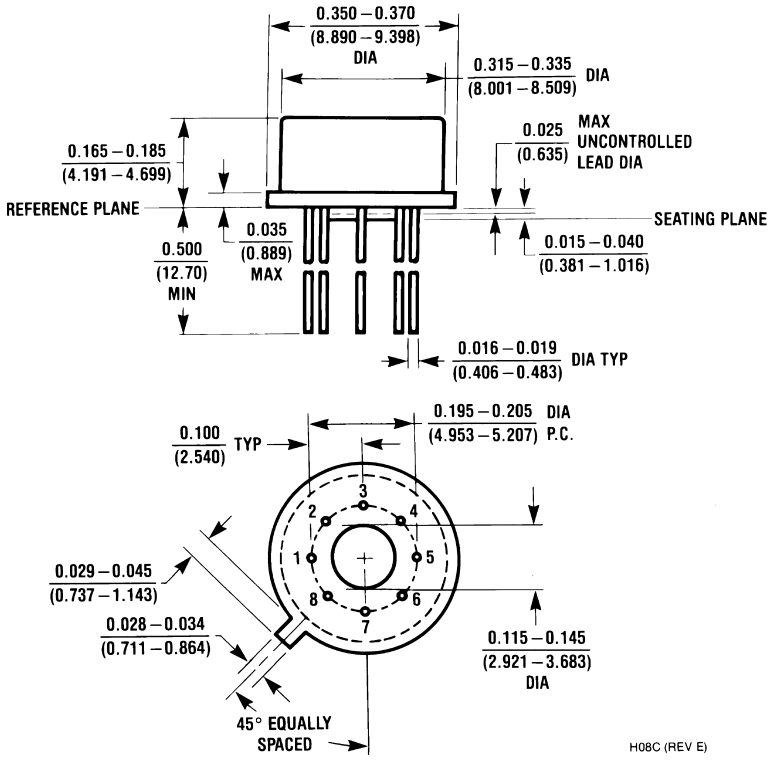
Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Schematic Diagram



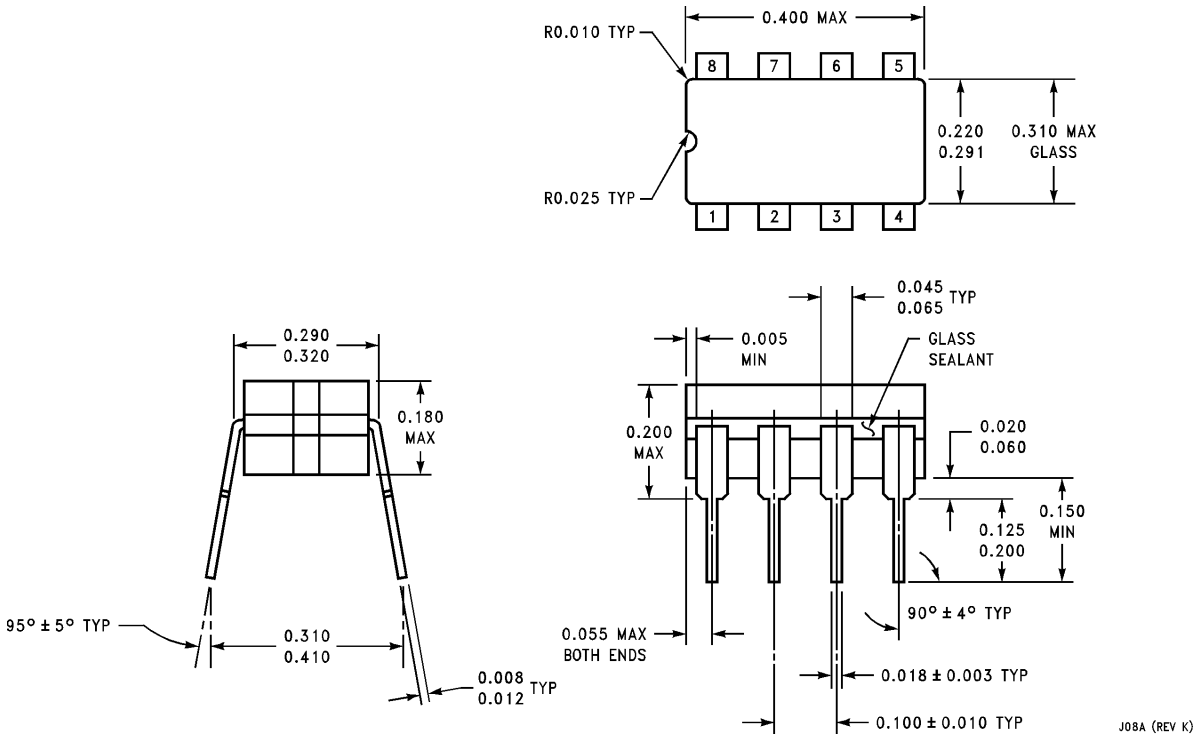
Physical Dimensions inches (millimeters)

unless otherwise noted

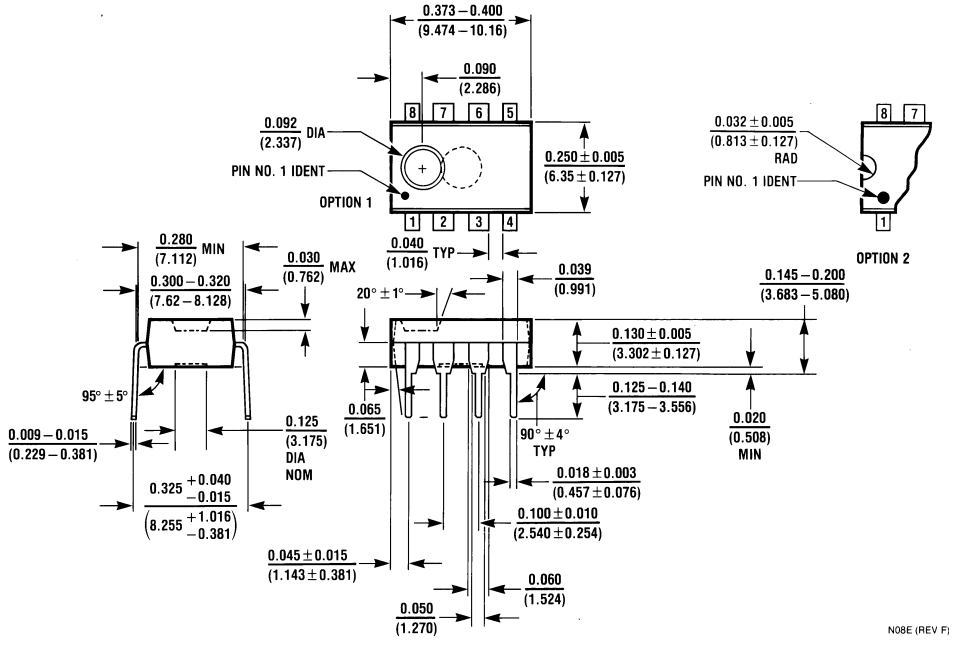


Metal Can Package (H)
Order Number LM741H, LM741H/883, LM741AH/883, LM741AH-MIL or LM741CH
NS Package Number H08C

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

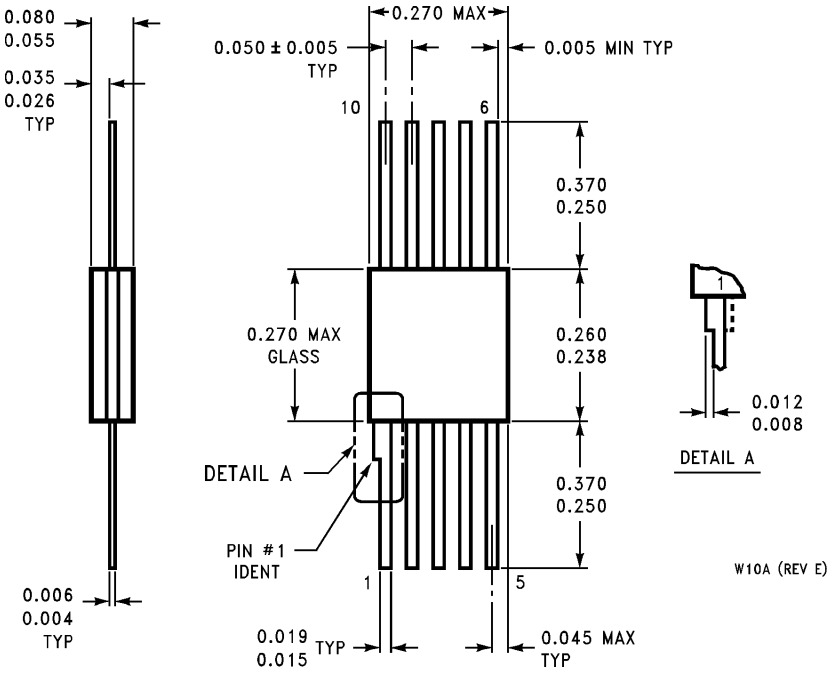


Ceramic Dual-In-Line Package (J)
Order Number LM741J/883
NS Package Number J08A



Dual-In-Line Package (N)
Order Number LM741CN
NS Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



10-Lead Ceramic Flatpak (W)
Order Number LM741W/883, LM741WG-MPR or LM741WG/883
NS Package Number W10A

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DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT00
Quad 2-input NAND gate

Product specification
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

Quad 2-input NAND gate 74HC/HCT00

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT00 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT00 provide the 2-input NAND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	7	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	22	22	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

Quad 2-input NAND gate 74HC/HCT00

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

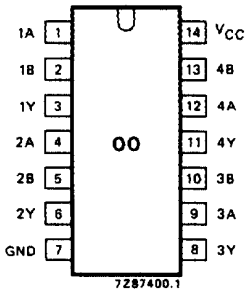


Fig.1 Pin configuration.

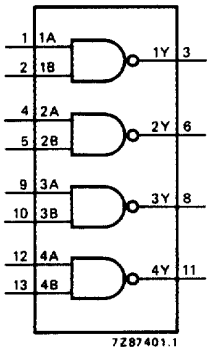


Fig.2 Logic symbol.

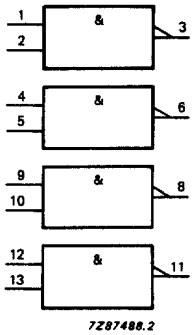


Fig.3 IEC logic symbol.

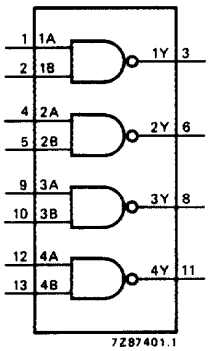


Fig.4 Functional diagram.

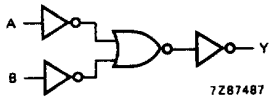


Fig.5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

Note

1. H = HIGH voltage level
   L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

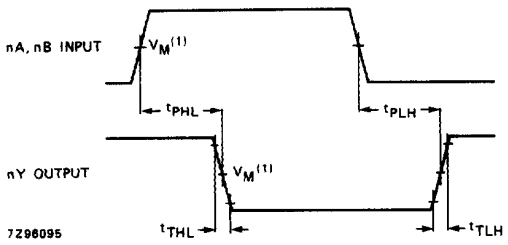
INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		12	19		24		29	ns	4.5	Fig.6
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6

AC WAVEFORMS



HC : V_M = 50%; V_I = GND to V_{CC}
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

DATA SHEET

74HC74; 74HCT74

Dual D-type flip-flop with set and reset; positive-edge trigger

Product specification
Supersedes data of 1998 Feb 23

2003 Jul 10

Philips
Semiconductors

PHILIPS

Dual D-type flip-flop with set and reset; positive-edge trigger

74HC74; 74HCT74

FEATURES

- Wide supply voltage range from 2.0 to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.

GENERAL DESCRIPTION

The 74HC/HCT74 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT74 are dual positive-edge triggered, D-type flip-flops with individual data (D) inputs, clock (CP) inputs, set ($\overline{SD}$) and reset ($\overline{RD}$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	nCP to nQ, n$\overline{Q}$		14	15	ns
	n$\overline{SD}$ to nQ, n$\overline{Q}$		15	18	ns
	n$\overline{RD}$ to nQ, n$\overline{Q}$		16	18	ns
f_{max}	maximum clock frequency		76	59	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	24	29	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. For 74HC74 the condition is V_I = GND to V_{CC}.
   For 74HCT74 the condition is V_I = GND to V_{CC} – 1.5 V.

FUNCTION TABLES

Table 1 See note 1

INPUT				OUTPUT	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Table 2 See note 1

INPUT				OUTPUT	
$\overline{SD}$	$\overline{RD}$	CP	D	Qn+1	$\overline{Q}$n+1
H	H	↑	L	L	H
H	H	↑	H	H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   ↑ = LOW-to-HIGH CP transition;
   Qn+1 = state after the next LOW-to-HIGH CP transition.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC74N	–40 to +125 °C	14	DIP14	plastic	SOT27-1
74HCT74N	–40 to +125 °C	14	DIP14	plastic	SOT27-1
74HC74D	–40 to +125 °C	14	SO14	plastic	SOT108-1
74HCT74D	–40 to +125 °C	14	SO14	plastic	SOT108-1
74HC74DB	–40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HCT74DB	–40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HC74PW	–40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HCT74PW	–40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HC74BQ	–40 to +125 °C	14	DHVQFN14	plastic	SOT762-1
74HCT74BQ	–40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	$1\overline{R}D$	asynchronous reset-direct input (active LOW)
2	1D	data input
3	1CP	clock input (LOW-to-HIGH, edge-triggered)
4	$1\overline{S}D$	asynchronous set-direct input (active LOW)
5	1Q	true flip-flop output
6	$1\overline{Q}$	complement flip-flop output
7	GND	ground (0 V)
8	$2\overline{Q}$	complement flip-flop output
9	2Q	true flip-flop output
10	$2\overline{S}D$	asynchronous set-direct input (active LOW)
11	2CP	clock input (LOW-to-HIGH, edge-triggered)
12	2D	data input
13	$2\overline{R}D$	asynchronous reset-direct input (active LOW)
14	V_{CC}	positive supply voltage

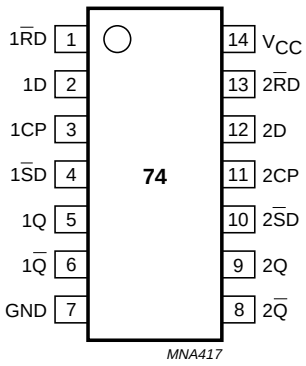
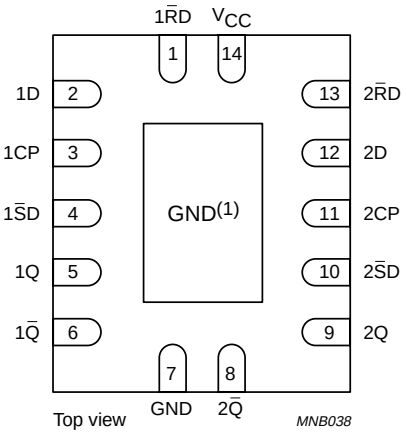


Fig.1 Pin configuration DIP14, SO14 and (T)SSOP14.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

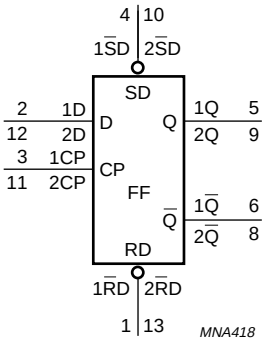


Fig.3 Logic symbol.

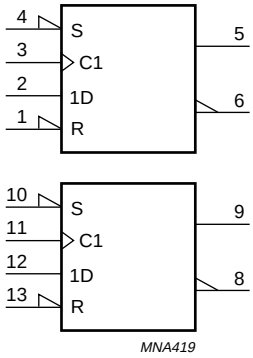


Fig.4 IEC logic symbol.

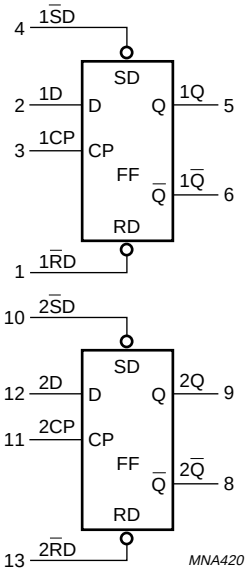


Fig.5 Functional diagram.

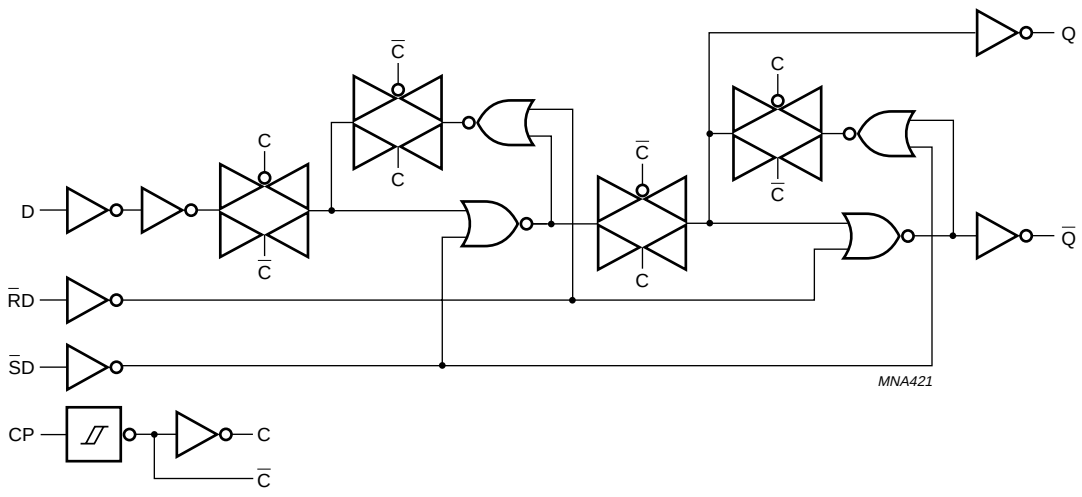


Fig.6 Logic diagram (one flip-flop).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC74			74HCT74			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature		–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	–	–	1000	–	–	500	ns
		V_{CC} = 4.5 V	–	6.0	500	–	6.0	500	ns
		V_{CC} = 6.0 V	–	–	400	–	–	500	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V; note 1	–	±20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V; note 1	–	±20	mA
I_O	output source or sink current	-0.5 V $< V_O < V_{CC} + 0.5$ V; note 1	–	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO14 packages: above 70 °C derate linearly with 8 mW/K.
   For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
   For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.
   For DIP14 packages: above 70 °C derate linearly with 12 mW/K.

DC CHARACTERISTICS

Family 74HC

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V_{IL}	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –4.0 mA	4.5	3.84	4.32	–	V
		I_O = –5.2 mA	6.0	5.34	5.81	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 4.0 mA	4.5	–	0.15	0.33	V
		I_O = 5.2 mA	6.0	–	0.16	0.33	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	6.0	–	–	±1.0	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	6.0	–	–	40	µA
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –4.0 mA	4.5	3.7	–	–	V
		I_O = –5.2 mA	6.0	5.2	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 4.0 mA	4.5	–	–	0.4	V
		I_O = 5.2 mA	6.0	–	–	0.4	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	6.0	–	–	±1.0	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	6.0	–	–	80	µA

Note

1. All typical values are measured at T_{amb} = 25 °C.

Family 74HCT

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; I_O = –4.0 mA	4.5	3.84	4.32	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; I_O = 4.0 mA	4.5	0.33	0.15	–	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	±1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	40	μA
ΔI_{CC}	additional quiescent supply current per input	V_I = V_{CC} –2.1 V other inputs at V_{CC} or GND; I_O = 0	4.5 to 5.5	–	100	450	μA
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; I_O = –4.0 mA	4.5	3.7	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; I_O = 4.0 mA	4.5	–	–	0.4	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	±1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	80	μA
ΔI_{CC}	additional quiescent supply current per input	V_I = V_{CC} –2.1 V other inputs at V_{CC} or GND; I_O = 0	4.5 to 5.5	–	–	490	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

Remark to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table.

INPUT	UNIT LOAD COEFFICIENT
nD	0.70
n$\overline{R}$D	0.70
n$\overline{S}$D	0.80
nCP	0.80

AC CHARACTERISTICS

Family 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$	see Fig.7	2.0	–	47	220	ns
			4.5	–	17	44	ns
			6.0	–	14	37	ns
	propagation delay n$\overline{SD}$ to nQ, n$\overline{Q}$	see Fig.8	2.0	–	50	250	ns
			4.5	–	18	50	ns
			6.0	–	14	43	ns
	propagation delay n$\overline{RD}$ to nQ, n$\overline{Q}$	see Fig.8	2.0	–	52	250	ns
			4.5	–	19	50	ns
			6.0	–	15	43	ns
t_{THL}/t_{TLH}	output transition time	see Fig.7	2.0	–	19	95	ns
			4.5	–	7	19	ns
			6.0	–	6	16	ns
t_W	clock pulse width HIGH or LOW	see Fig.7	2.0	100	19	–	ns
			4.5	20	7	–	ns
			6.0	17	6	–	ns
	set or reset pulse width LOW	see Fig.8	2.0	100	19	–	ns
			4.5	20	7	–	ns
			6.0	17	6	–	ns
t_{rem}	removal time set or reset	see Fig.8	2.0	40	3	–	ns
			4.5	8	1	–	ns
			6.0	7	1	–	ns
t_{su}	set-up time nD to nCP	see Fig.7	2.0	75	6	–	ns
			4.5	15	2	–	ns
			6.0	13	2	–	ns
t_h	hold time nCP to nD	see Fig.7	2.0	3	–6	–	ns
			4.5	3	–2	–	ns
			6.0	3	–2	–	ns
f_{max}	maximum clock pulse frequency	see Fig.7	2.0	4.8	23	–	MHz
			4.5	24	69	–	MHz
			6.0	28	82	–	MHz

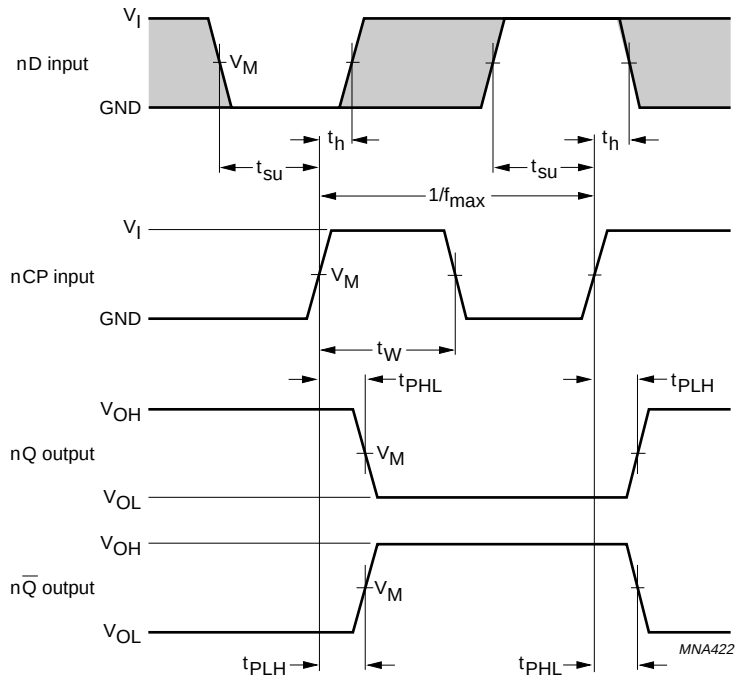
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$	see Fig.7	2.0	–	–	265	ns
			4.5	–	–	53	ns
			6.0	–	–	45	ns
	propagation delay n$\overline{SD}$ to nQ, n$\overline{Q}$	see Fig.8	2.0	–	–	300	ns
			4.5	–	–	60	ns
			6.0	–	–	51	ns
	propagation delay n$\overline{RD}$ to nQ, n$\overline{Q}$	see Fig.8	2.0	–	–	300	ns
			4.5	–	–	60	ns
			6.0	–	–	51	ns
t_{THL}/t_{TLH}	output transition time	see Fig.7	2.0	–	–	110	ns
			4.5	–	–	22	ns
			6.0	–	–	19	ns
t_W	clock pulse width HIGH or LOW	see Fig.7	2.0	120	–	–	ns
			4.5	24	–	–	ns
			6.0	20	–	–	ns
t_W	set or reset pulse width LOW	see Fig.8	2.0	120	–	–	ns
			4.5	24	–	–	ns
			6.0	20	–	–	ns
t_{rem}	removal time set or reset	see Fig.8	2.0	45	–	–	ns
			4.5	9	–	–	ns
			6.0	8	–	–	ns
t_{su}	set-up time nD to nCP	see Fig.7	2.0	90	–	–	ns
			4.5	18	–	–	ns
			6.0	15	–	–	ns
t_h	hold time nCP to nD	see Fig.7	2.0	3	–	–	ns
			4.5	3	–	–	ns
			6.0	3	–	–	ns
f_{max}	maximum clock pulse frequency	see Fig.7	2.0	4.0	–	–	MHz
			4.5	20	–	–	MHz
			6.0	24	–	–	MHz

Family 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

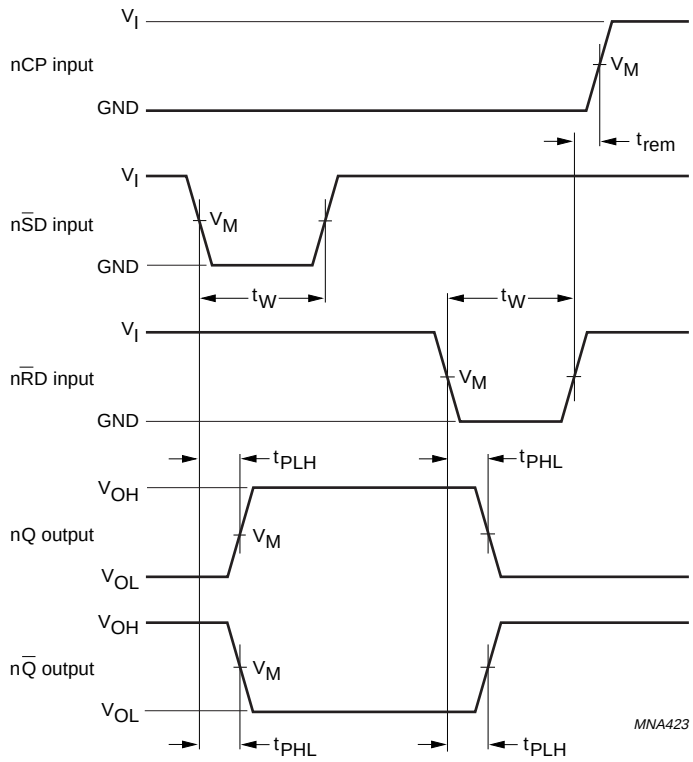
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$	see Fig.7	4.5	–	18	44	ns
	propagation delay n$\overline{S}$D to nQ, n$\overline{Q}$	see Fig.8	4.5	–	23	50	ns
	propagation delay n$\overline{R}$D to nQ, n$\overline{Q}$	see Fig.8	4.5	–	24	50	ns
t_{THL}/t_{TLH}	output transition time	see Fig.7	4.5	–	7	19	ns
t_W	clock pulse width HIGH or LOW	see Fig.7	4.5	23	9	–	ns
	set or reset pulse width LOW	see Fig.8	4.5	20	9	–	ns
t_{rem}	removal time set or reset	see Fig.8	4.5	8	1	–	ns
t_{su}	set-up time nD to nCP	see Fig.7	4.5	15	5	–	ns
t_h	hold time nCP to nD	see Fig.7	4.5	+3	–3	–	ns
f_{max}	maximum clock pulse frequency	see Fig.7	4.5	22	54	–	MHz
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$	see Fig.7	4.5	–	–	53	ns
	propagation delay n$\overline{S}$D to nQ, n$\overline{Q}$	see Fig.8	4.5	–	–	60	ns
	propagation delay n$\overline{R}$D to nQ, n$\overline{Q}$	see Fig.8	4.5	–	–	60	ns
t_{THL}/t_{TLH}	output transition time	see Fig.7	4.5	–	–	22	ns
t_W	clock pulse width HIGH or LOW	see Fig.7	4.5	27	–	–	ns
	set or reset pulse width LOW	see Fig.8	4.5	24	–	–	ns
t_{rem}	removal time set or reset	see Fig.8	4.5	9	–	–	ns
t_{su}	set-up time nD to nCP	see Fig.7	4.5	18	–	–	ns
t_h	hold time nCP to nD	see Fig.7	4.5	3	–	–	ns
f_{max}	maximum clock pulse frequency	see Fig.7	4.5	18	–	–	MHz

AC WAVEFORMS



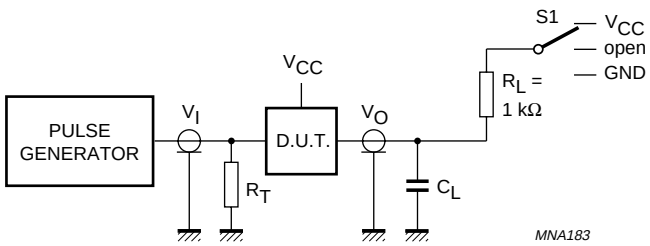
The shaded areas indicate when the input is permitted to change for predictable output performance.
74HC74: V_M = 50%; V_I = GND to V_{CC}.
74HCT74: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 The clock (nCP) to output (nQ, n$\overline{Q}$) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency.



74HC74: V_M = 50%; V_I = GND to V_{CC}.
74HCT74: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 The set ($n\overline{S}D$) and reset ($n\overline{R}D$) input to output (nQ, $n\overline{Q}$) propagation delays, the set and reset pulse widths and the $n\overline{R}D$, $n\overline{R}D$ to nCP removal time.



TEST	S1
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}

Definitions for test circuit:

R_L = Load resistor.

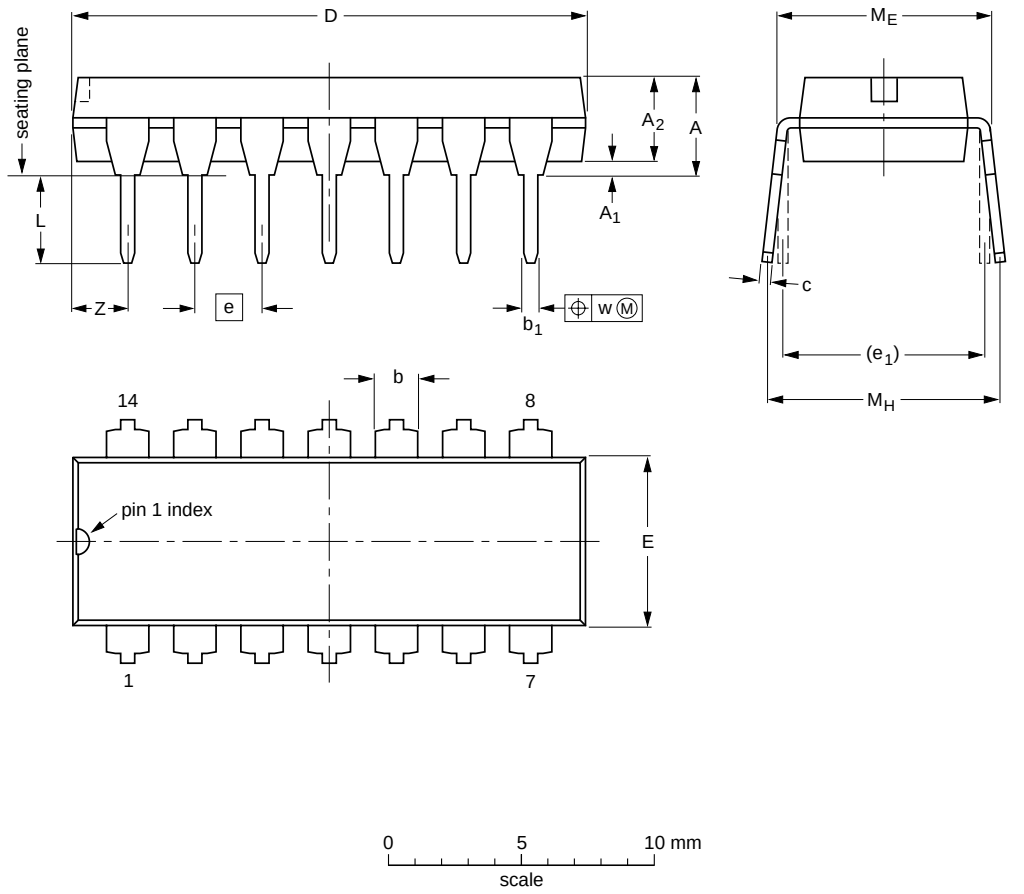
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.9 Load circuitry for switching times.

PACKAGE OUTLINES

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

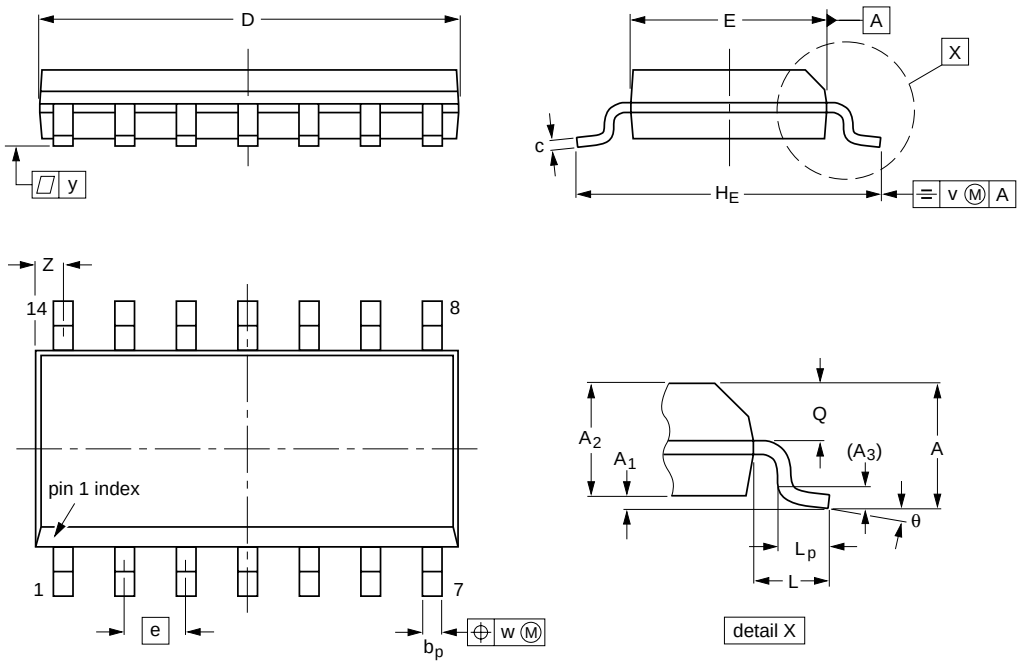
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

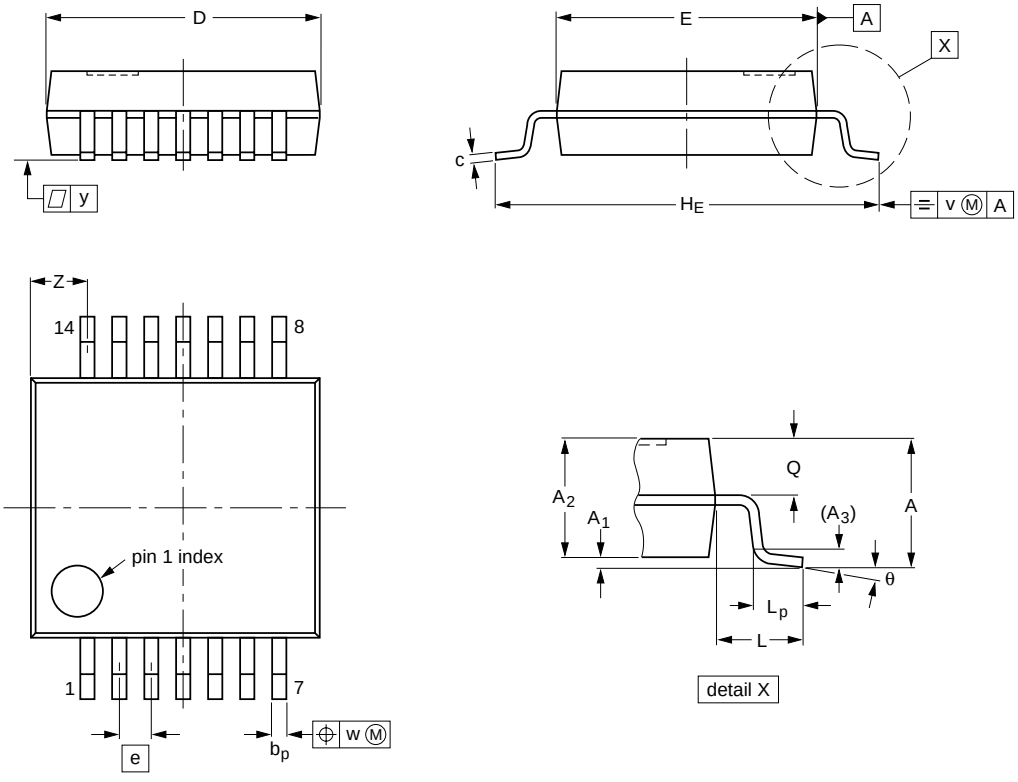
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

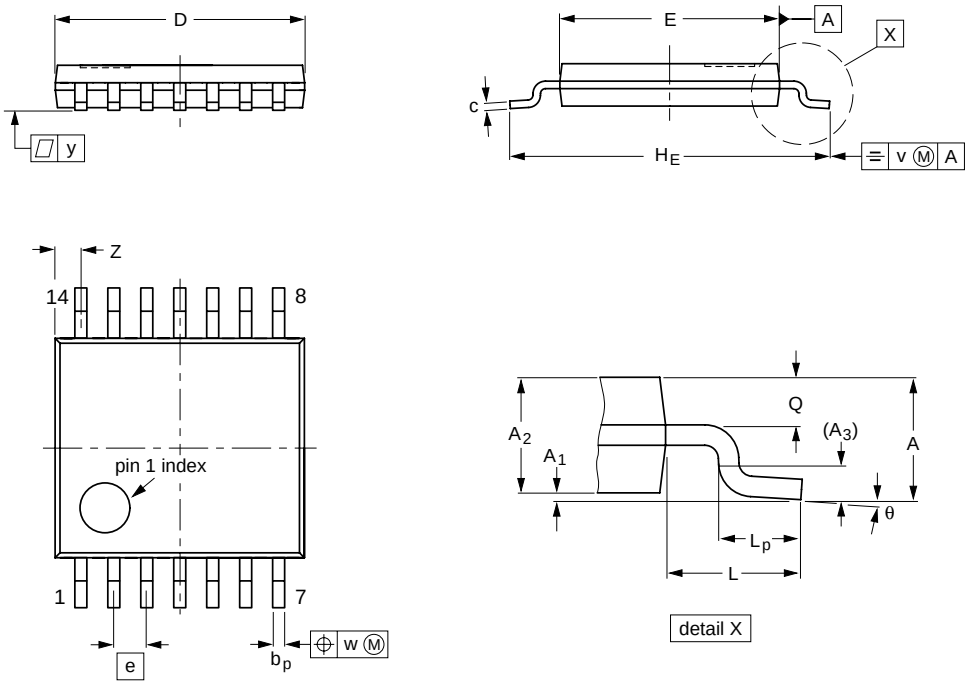
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

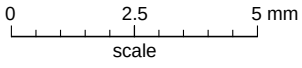
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**





DIMENSIONS (mm are the original dimensions)

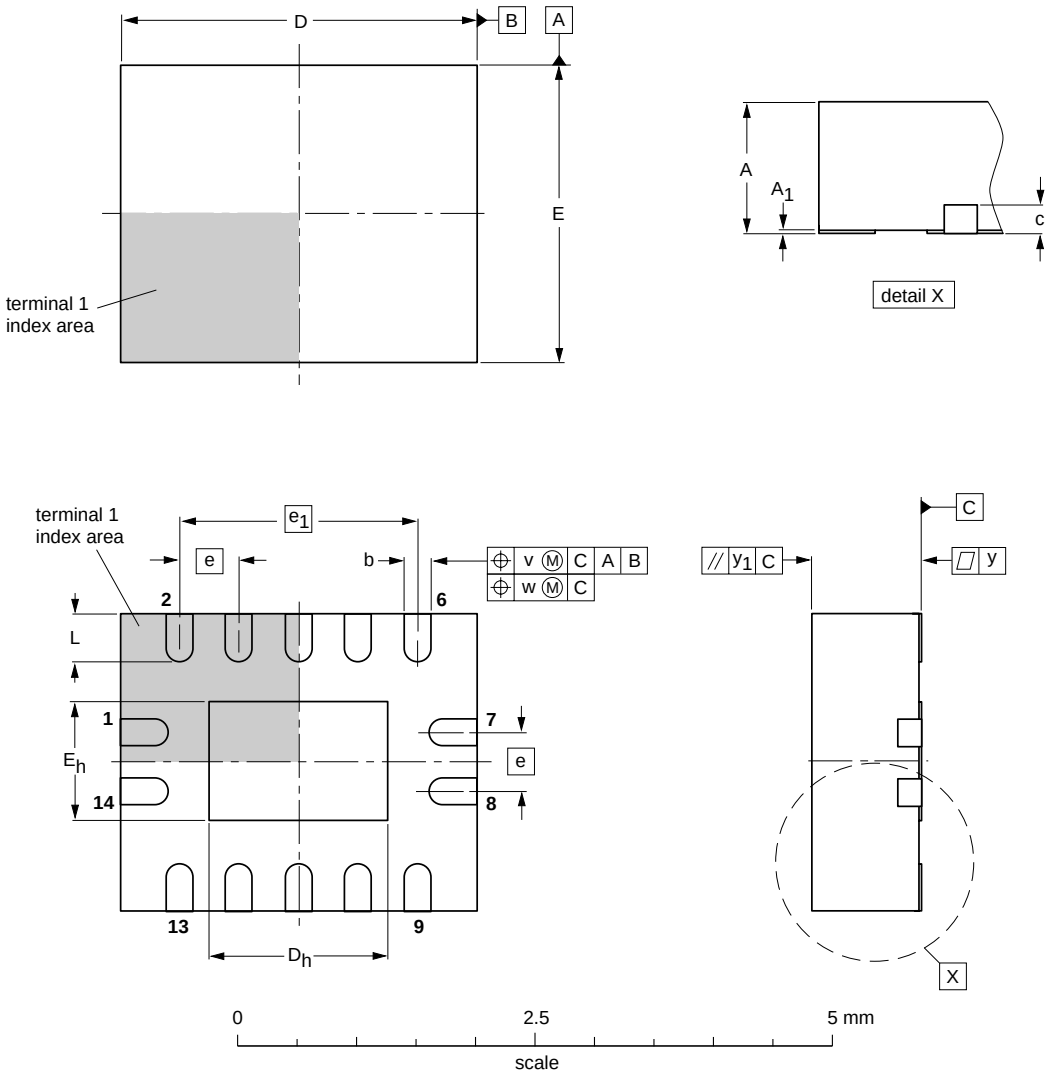
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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MOTOROLA

SN54/74LS112A

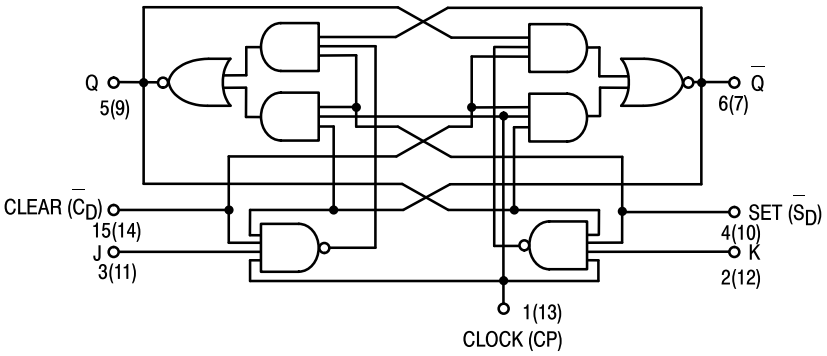
DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

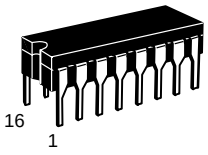
The SN54/74LS112A dual JK flip-flop features individual J, K, clock, and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

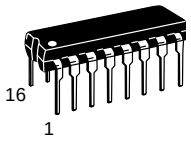
LOW POWER SCHOTTKY

LOGIC DIAGRAM (Each Flip-Flop)

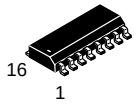




J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

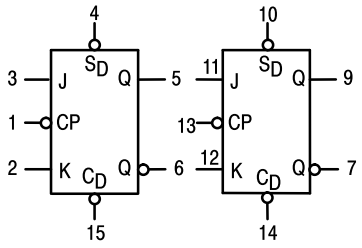
MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S_D}$	$\overline{C_D}$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	q	q
Load “0” (Reset)	H	H	l	h	L	H
Load “1” (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	q

* Both outputs will be HIGH while both S_D and C_D are LOW, but the output states are unpredictable if S_D and C_D go HIGH simultaneously.

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don’t Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current	J, K Set, Clear Clock			20 60 80	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		J, K Set, Clear Clock			0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	J, K Clear, Set, Clk			−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				6.0	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

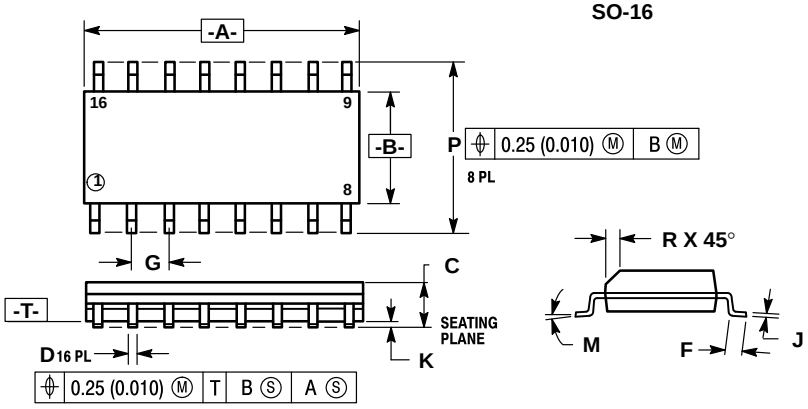
AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	30	45		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock Clear, Set to Output		15	20	ns	
			15	20	ns	

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_W	Clock Pulse Width High	20			ns	V_{CC} = 5.0 V
t_W	Clear, Set Pulse Width	25			ns	
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

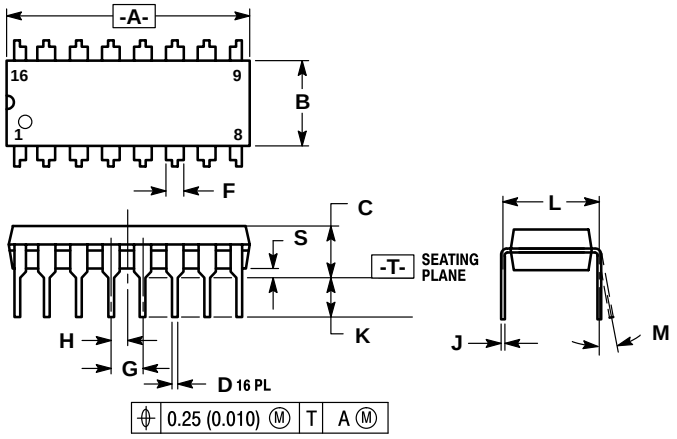
Case 751B-03 D Suffix
16-Pin Plastic
SO-16



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

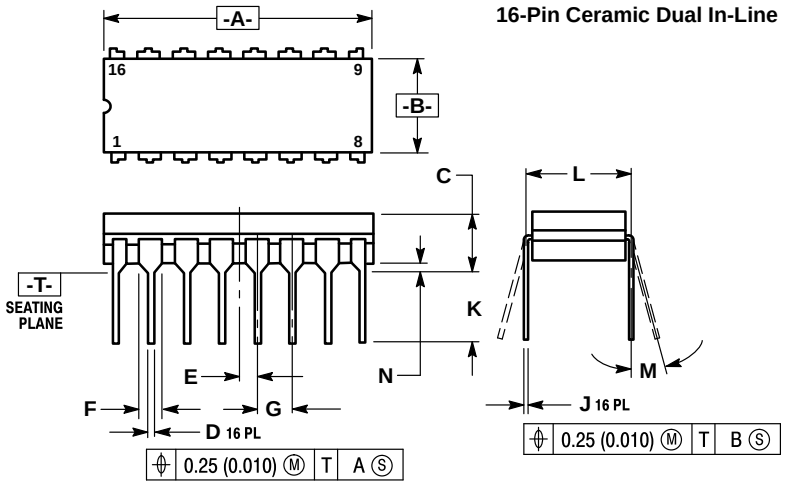
Case 648-08 N Suffix
16-Pin Plastic



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

Case 620-09 J Suffix
16-Pin Ceramic Dual In-Line



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

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EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT175
Quad D-type flip-flop with reset; positive-edge trigger

Product specification
Supersedes data of December 1990
File under Integrated Circuits, IC06

1998 Jul 08

Philips Semiconductors

PHILIPS

Quad D-type flip-flop with reset; positive-edge trigger 74HC/HCT175

FEATURES

- Four edge-triggered D flip-flops
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT175 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT175 have four edge-triggered, D-type flip-flops with individual D inputs and both Q and $\overline{Q}$ outputs.
The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.
The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All Q_n outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where both the true and complement outputs are required and the clock and master reset are common to all storage elements.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	CP to Q_n, $\overline{Q}_n$		17	16	ns
	$\overline{MR}$ to Q_n		15	19	ns
t_{PLH}	propagation delay				
	CP to Q_n, $\overline{Q}_n$		17	16	ns
	$\overline{MR}$ to $\overline{Q}_n$		15	16	ns
f_{max}	maximum clock frequency		83	54	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	32	34	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
74HC175N; 74HCT175N	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HC175D; 74HCT175D	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC175DB; 74HCT175DB	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC175PW; 74HCT175PW	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2, 7, 10, 15	Q_0 to Q_3	flip-flop outputs
3, 6, 11, 14	$\overline{Q}_0$ to $\overline{Q}_3$	complementary flip-flop outputs
4, 5, 12, 13	D_0 to D_3	data inputs
8	GND	ground (0 V)
9	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

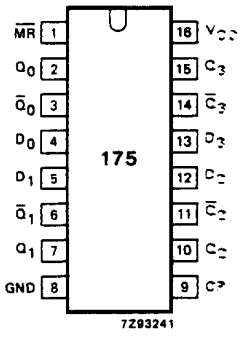


Fig.1 Pin configuration.

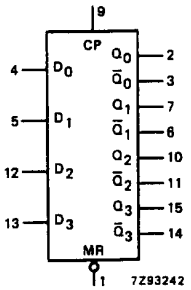


Fig.2 Logic symbol.

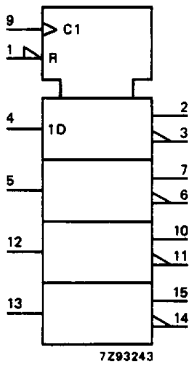


Fig.3 IEC logic symbol.

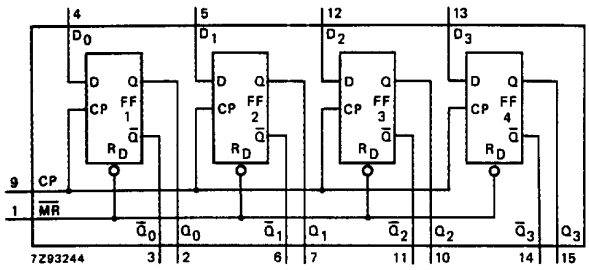


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
reset (clear)	L	X	X	L	H
load “1”	H	↑	h	H	L
load “0”	H	↑	I	L	H

Note

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level
   I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
   ↑ = LOW-to-HIGH CP transition
   X = don’t care

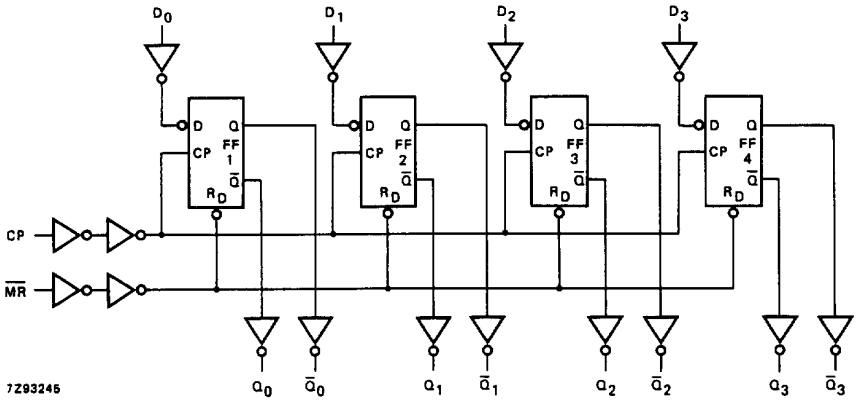


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n, $\overline{Q}_n$		55	175		220		265	ns	2.0	Fig.6
			20	35		44		53		4.5	
			16	30		37		45		6.0	
t_{PHL}/ t_{PLH}	propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$		50	150		190		225	ns	2.0	Fig.8
			18	30		38		45		4.5	
			14	26		33		38		6.0	
t_{THL}/ t_{TLH}	output transition time		19	75		95		110	ns	2.0	Fig.6
			7	15		19		22		4.5	
			6	13		16		19		6.0	
t_W	clock pulse width HIGH or LOW	80	22		100		120		ns	2.0	Fig.6
		16	8		20		24			4.5	
		14	6		17		20			6.0	
t_W	master reset pulse width LOW	80	19		100		120		ns	2.0	Fig.8
		16	7		20		24			4.5	
		14	6		17		20			6.0	
t_{rem}	removal time $\overline{MR}$ to CP	5	–33		5		5		ns	2.0	Fig.8
		5	–12		5		5			4.5	
		5	–10		5		5			6.0	
t_{su}	set-up time D_n to CP	80	3		100		120		ns	2.0	Fig.7
		16	1		20		24			4.5	
		14	1		17		20			6.0	
t_h	hold time CP to D_n	25	2		30		40		ns	2.0	Fig.7
		5	0		6		8			4.5	
		4	0		5		7			6.0	
f_{max}	maximum clock pulse frequency	6.0	25		4.8		4.0		MHz	2.0	Fig.6
		30	75		24		20			4.5	
		35	89		28		24			6.0	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

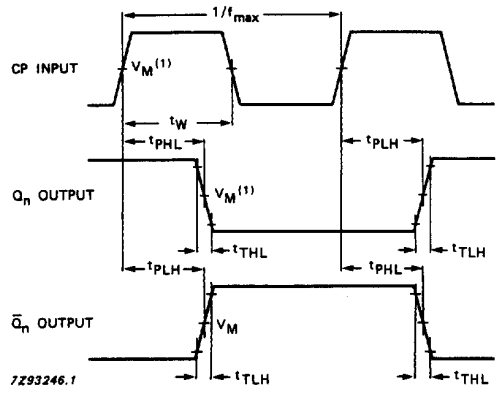
INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	1.00
CP	0.60
D_n	0.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

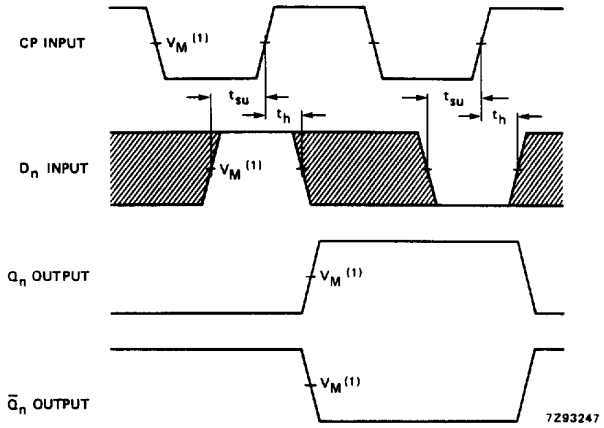
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n, $\overline{Q}_n$		19	33		41		50	ns	4.5	Fig.6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		22	38		48		57	ns	4.5	Fig.8
t_{PLH}	propagation delay $\overline{MR}$ to $\overline{Q}_n$		19	35		44		53	ns	4.5	Fig.8
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6
t_W	clock pulse width HIGH or LOW	20	12		25		30		ns	4.5	Fig.6
t_W	master reset pulse width LOW	20	11		25		30		ns	4.5	Fig.8
t_{rem}	removal time $\overline{MR}$ to CP	5	−10		5		5		ns	4.5	Fig.8
t_{su}	set-up time D_n to CP	16	5		20		24		ns	4.5	Fig.7
t_h	hold time CP to D_n	5	0		5		5		ns	4.5	Fig.7
f_{max}	maximum clock pulse frequency	25	49		20		17		MHz	4.5	Fig.6

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

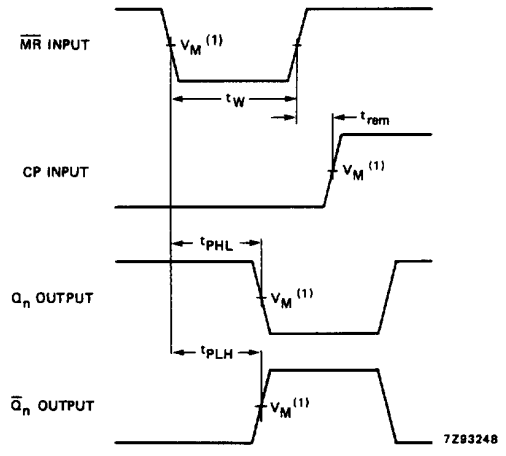
Fig.6 Waveforms showing the clock (CP) to outputs (Q_n, $\overline{Q}n$) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the data set-up and hold times for the data input (D_n).

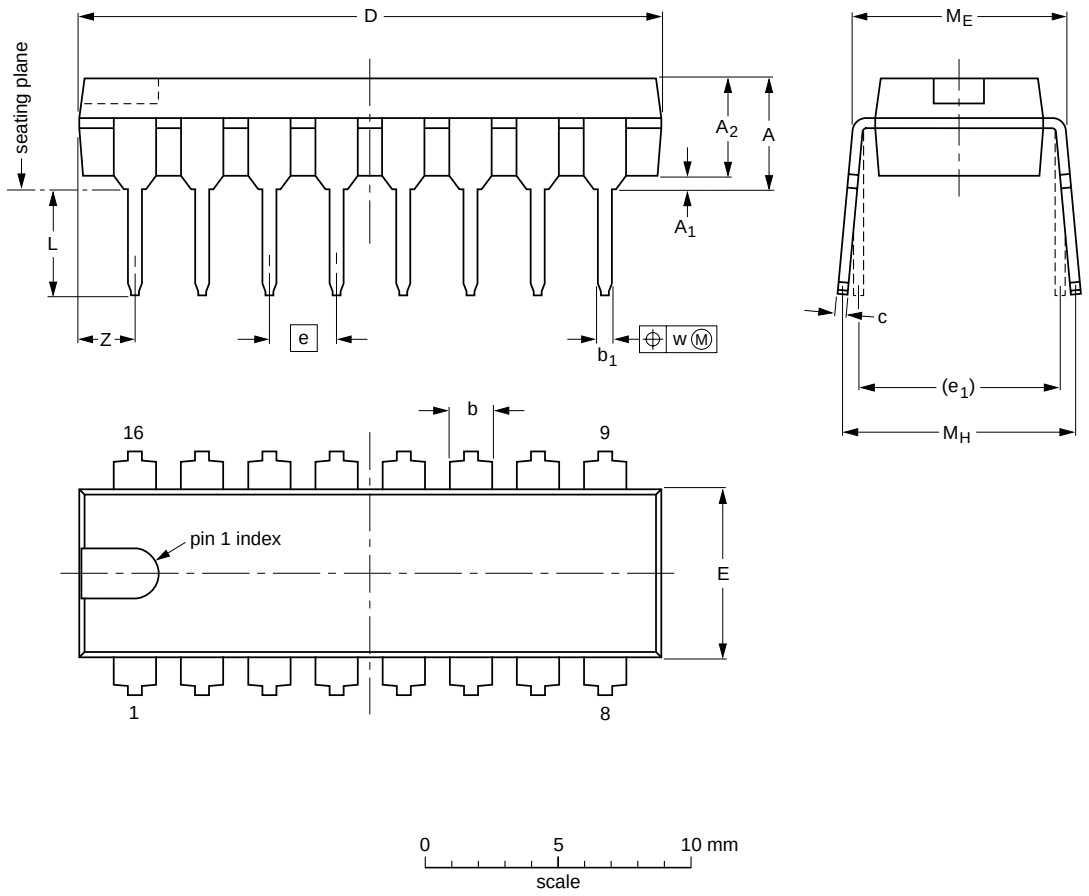


(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to outputs (Q_n, $\overline{Q}_n$) propagation delays and the master reset to clock (CP) removal time.

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

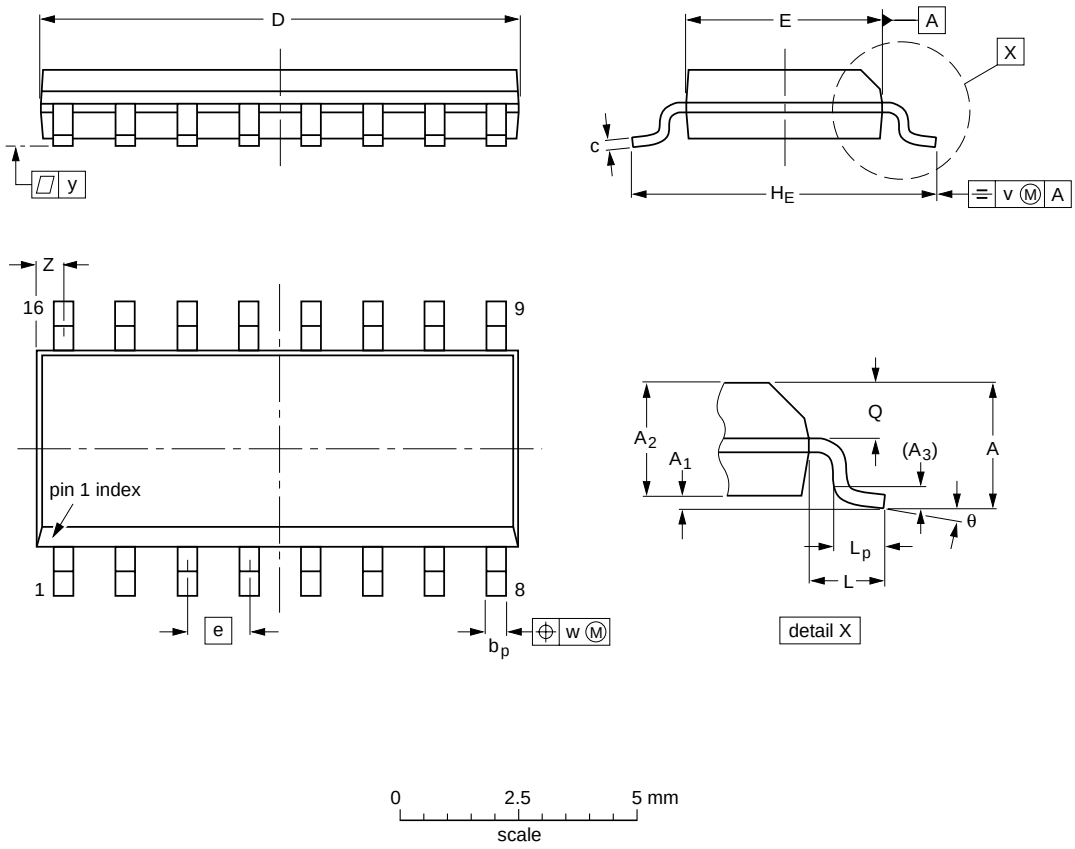
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

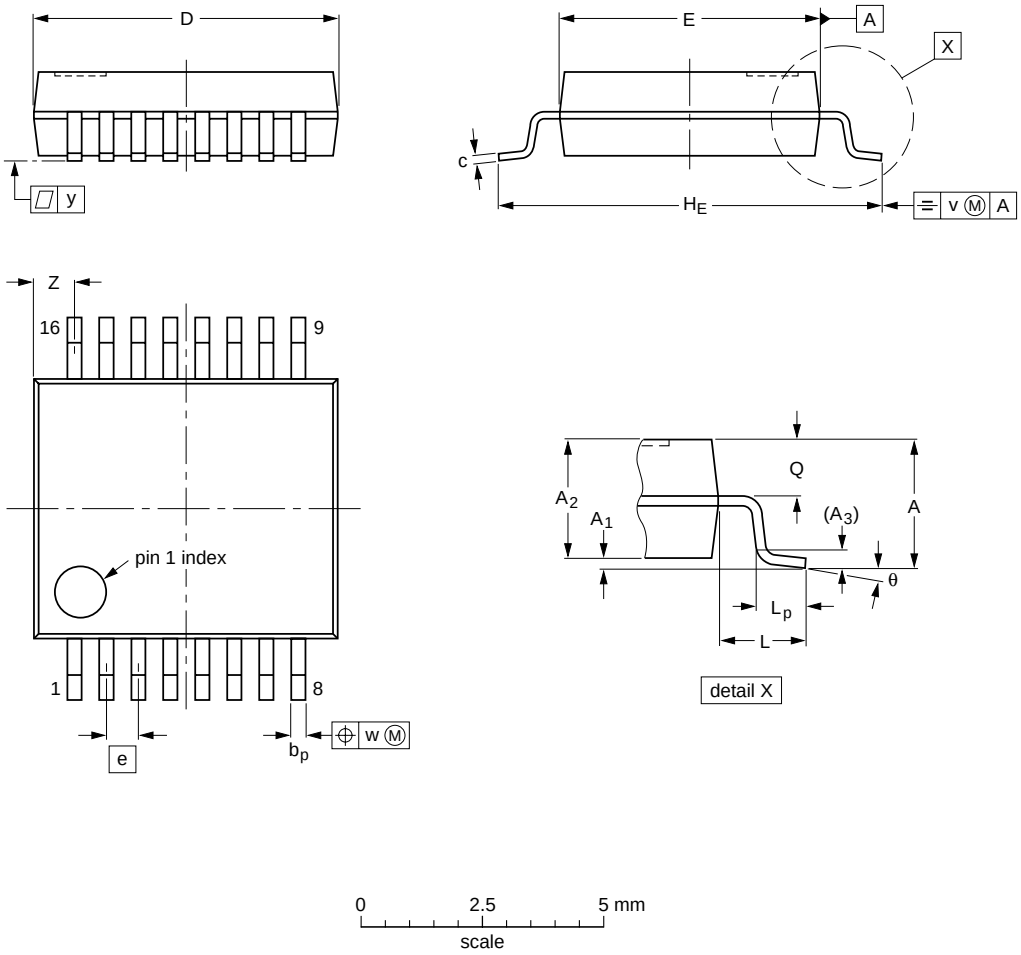
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

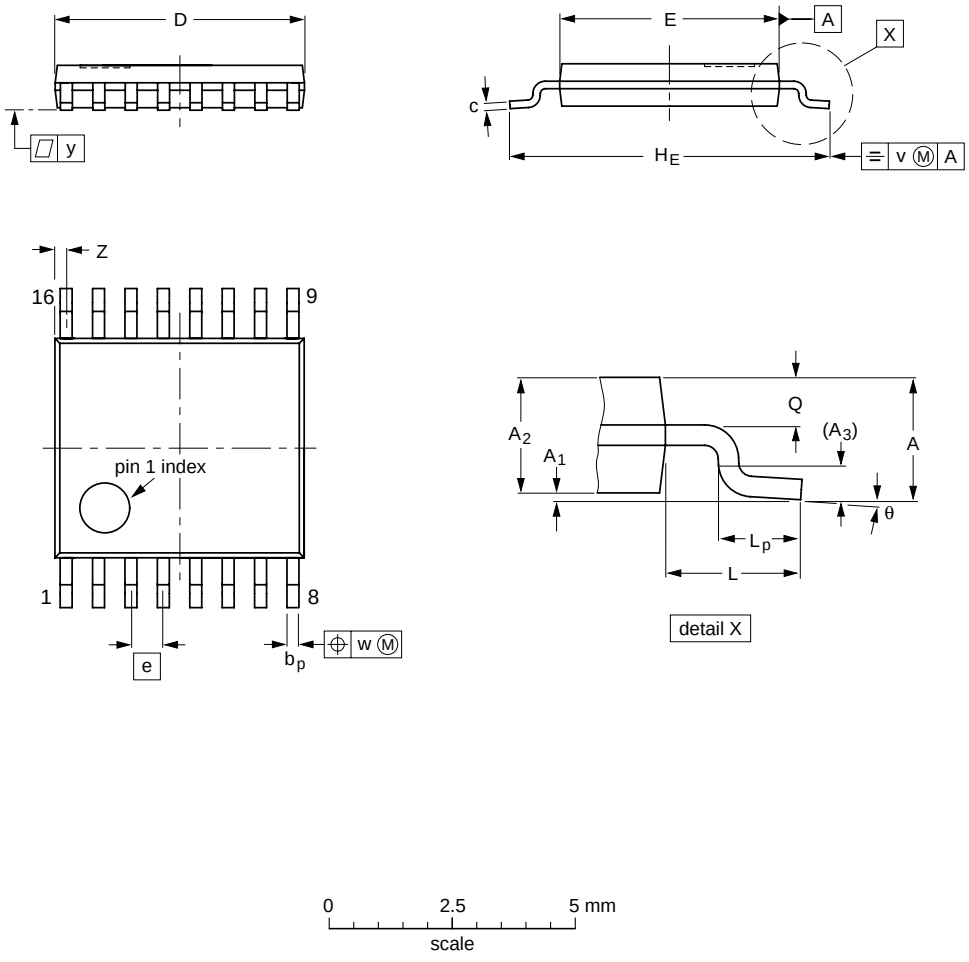
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO, SSOP and TSSOP

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO, SSOP and TSSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method.

Typical reflow temperatures range from 215 to 250 °C. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering can be used for all SO packages. Wave soldering is **not** recommended for SSOP and TSSOP packages, because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering is used - **and cannot be avoided for SSOP and TSSOP packages** - the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.

Even with these conditions:

- **Only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**
- **Do not consider wave soldering TSSOP packages with 48 leads or more, that is TSSOP48 (SOT362-1) and TSSOP56 (SOT364-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT08
Quad 2-input AND gate

Product specification
File under Integrated Circuits, IC06

December 1990

Philips
Semiconductors

PHILIPS

Quad 2-input AND gate 74HC/HCT08

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT08 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT08 provide the 2-input AND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	7	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	10	20	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} –1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

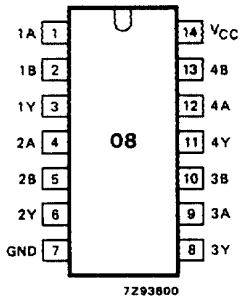


Fig.1 Pin configuration.

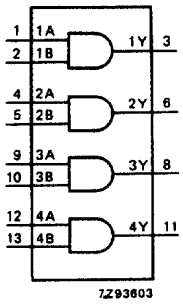


Fig.2 Logic symbol.

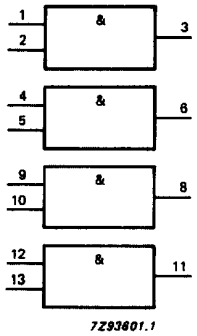


Fig.3 IEC logic symbol.

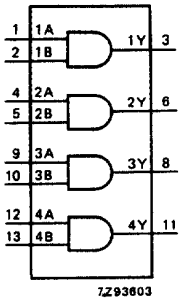


Fig.4 Functional diagram.

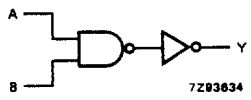


Fig.5 HC logic diagram (one gate).

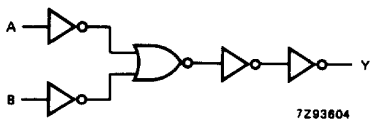


Fig.6 HCT logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

Note

1. H = HIGH voltage level
   L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

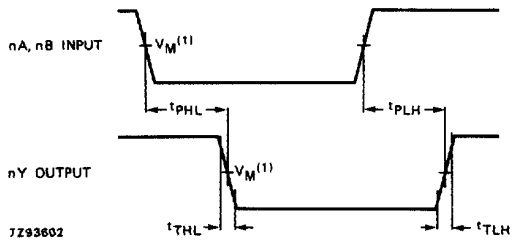
INPUT	UNIT LOAD COEFFICIENT
nA, nB	0.6

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		14	24		30		36	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.7

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

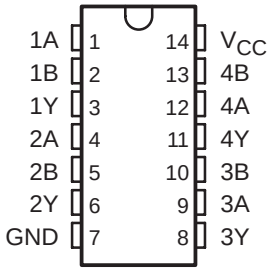
Fig.7 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

PACKAGE OUTLINES

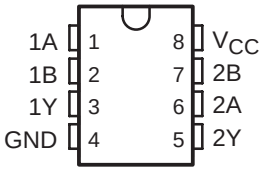
See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

- **Package Options Include Plastic Small-Outline (D, NS, PS), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**
- **Also Available as Dual 2-Input Positive-NAND Gate in Small-Outline (PS) Package**

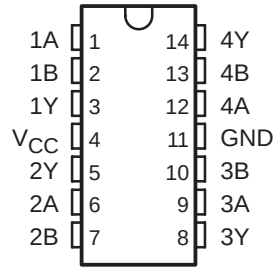
SN5400 . . . J PACKAGE
SN54LS00, SN54S00 . . . J OR W PACKAGE
SN7400, SN74S00 . . . D, N, OR NS PACKAGE
SN74LS00 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)



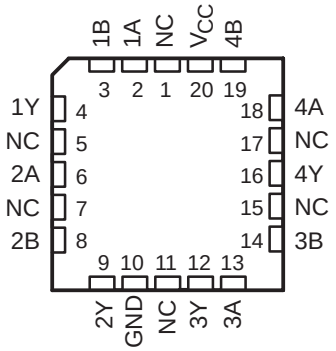
SN74LS00, SN74S00 . . . PS PACKAGE
(TOP VIEW)



SN5400 . . . W PACKAGE
(TOP VIEW)



SN54LS00, SN54S00 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

These devices contain four independent 2-input NAND gates. The devices perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

description/ordering information (continued)

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP − N	Tube	SN7400N	SN7400N
			SN74LS00N	SN74LS00N
			SN74S00N	SN74S00N
	SOIC − D	Tube	SN7400D	7400
		Tape and reel	SN7400DR	
		Tube	SN74LS00D	LS00
		Tape and reel	SN74LS00DR	
		Tube	SN74S00D	S00
		Tape and reel	SN74S00DR	
	SOP − NS	Tape and reel	SN7400NSR	SN7400
			SN74LS00NSR	74LS00
			SN74S00NSR	74S00
	SOP − PS	Tape and reel	SN74LS00PSR	LS00
			SN74S00PSR	S00
	SSOP − DB	Tape and reel	SN74LS00DBR	LS00
−55°C to 125°C	CDIP − J	Tube	SNJ5400J	SNJ5400J
			SNJ54LS00J	SNJ54LS00J
			SNJ54S00J	SNJ54S00J
	CFP − W	Tube	SNJ5400W	SNJ5400W
			SNJ54LS00W	SNJ54LS00W
			SNJ54S00W	SNJ54S00W
	LCCC − FK	Tube	SNJ54LS00FK	SNJ54LS00FK
			SNJ54S00FK	SNJ54S00FK

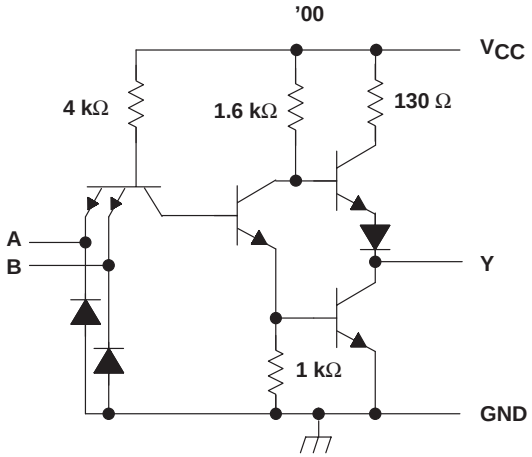
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

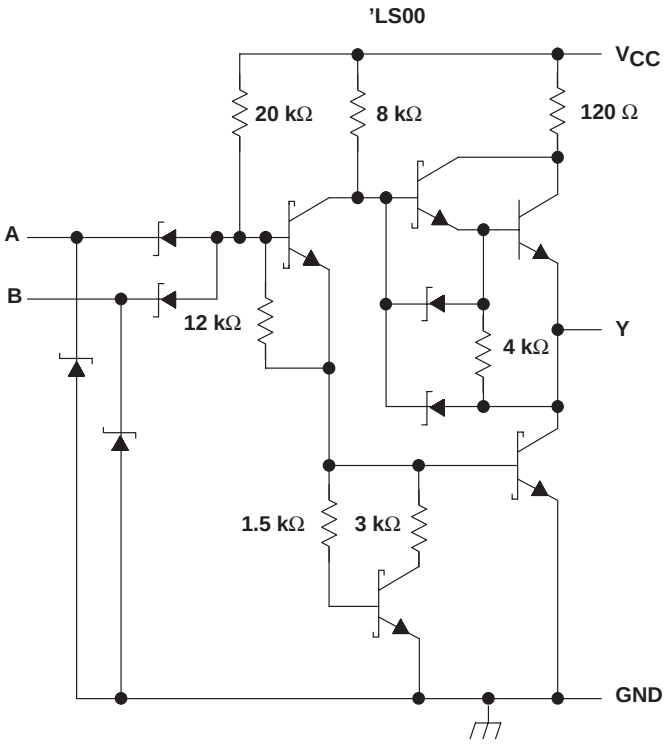
FUNCTION TABLE
(each gate)

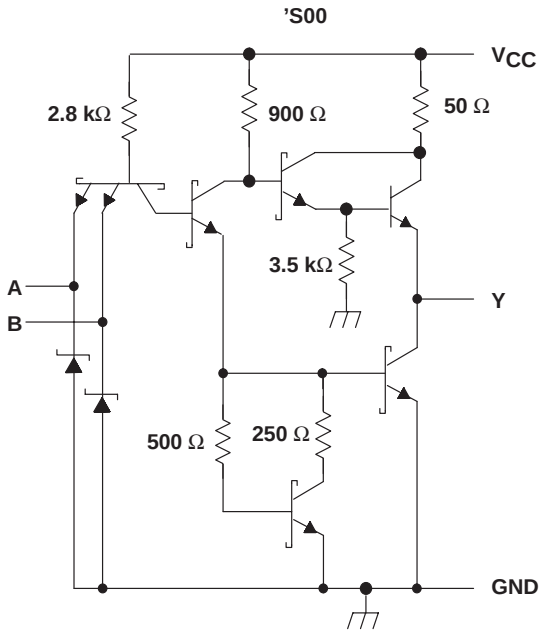
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic diagram, each gate (positive logic)

schematic







Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: ’00, ’S00 . . . . . 5.5 V
’LS00 . . . . . 7 V
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PS package . . . . . 95°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package termal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN5400			SN7400			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡			SN5400			SN7400			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}¶	V_{CC} = MAX			−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			4	8		4	8	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			12	22		12	22	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN5400 SN7400			UNIT
				MIN	TYP	MAX	
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		11	22	ns
t_{PHL}					7	15	

recommended operating conditions (see Note 4)

		SN54LS00			SN74LS00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS00			SN74LS00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8mA					0.35	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7V				20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			0.8	1.6		0.8	1.6	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			2.4	4.4		2.4	4.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS00 SN74LS00			UNIT
				MIN	TYP	MAX	
t_{PLH}	A or B	Y	R_L = 2 kΩ, C_L = 15 pF		9	15	ns
t_{PHL}					10	15	

recommended operating conditions (see Note 5)

		SN54S00			SN74S00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

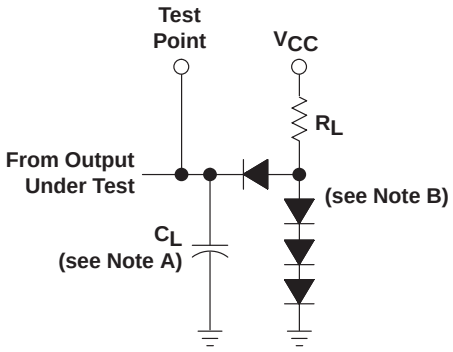
PARAMETER	TEST CONDITIONS†			SN54S00			SN74S00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				50			50	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.5V				−2			−2	mA
I_{OS}§	V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			10	16		10	16	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			20	36		20	36	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

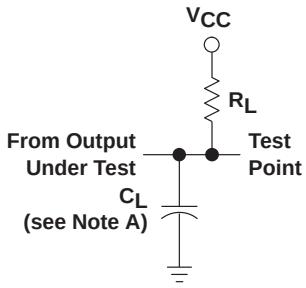
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		SN54S00 SN74S00			UNIT
					MIN	TYP	MAX	
t_{PLH}	A or B	Y	R_L = 280 Ω,	C_L = 15 pF		3	4.5	ns
t_{PHL}						3	5	
t_{PLH}	A or B	Y	R_L = 280 Ω,	C_L = 50 pF		4.5		ns
t_{PHL}						5		

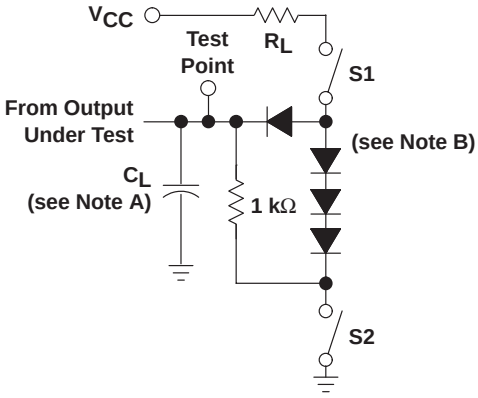
PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 DEVICES



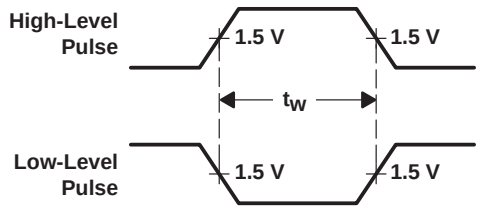
LOAD CIRCUIT FOR 2-STATE TOTEM-POLE OUTPUTS



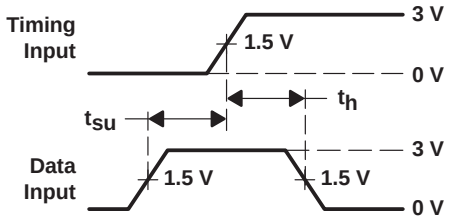
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



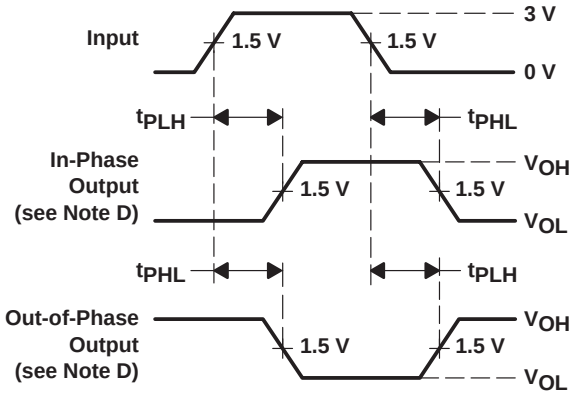
LOAD CIRCUIT FOR 3-STATE OUTPUTS



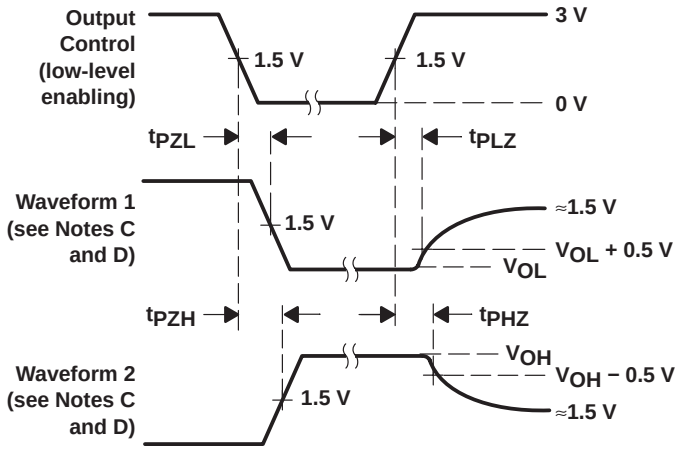
VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$; t_r and $t_f \le 7$ ns for Series 54/74 devices and t_r and $t_f \le 2.5$ ns for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
JM38510/00104BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
JM38510/00104BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/07001BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
JM38510/07001BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/30001B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/30001BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
JM38510/30001BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/30001SCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
JM38510/30001SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SN5400J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN54LS00J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN54S00J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN7400D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7400DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7400DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN7400N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7400N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7400NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS00D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS00DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74LS00DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS00DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS00DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS00DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS00DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS00DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS00DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS00DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS00J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS00N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS00NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74LS00NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS00NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS00PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS00PSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS00PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S00D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S00DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S00DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S00DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S00DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S00DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S00N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S00N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74S00NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S00NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S00NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S00NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ5400J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ5400W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ5400WA	OBSOLETE	CFP	WA	14		TBD	A42	N / A for Pkg Type
SNJ54LS00FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS00J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ54LS00W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54S00FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54S00J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ54S00W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

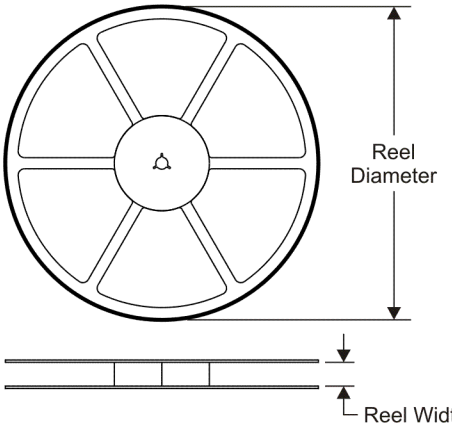
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

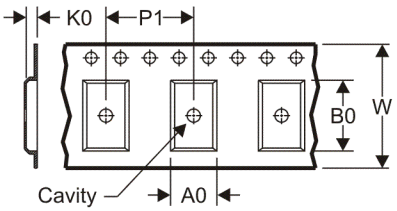
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

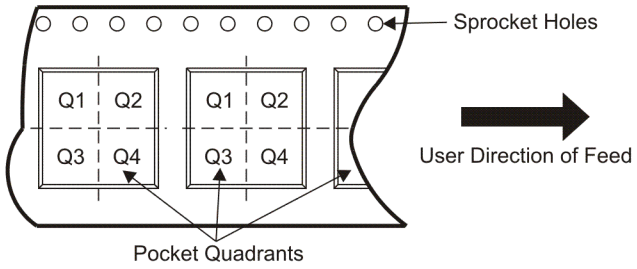


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

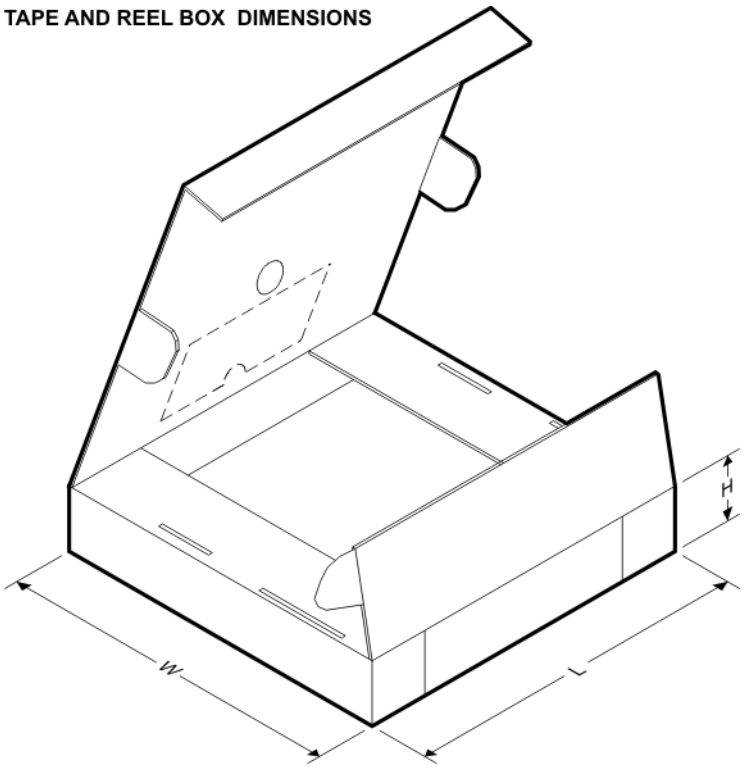
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS00DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LS00DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS00NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS00PSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74S00DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74S00NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



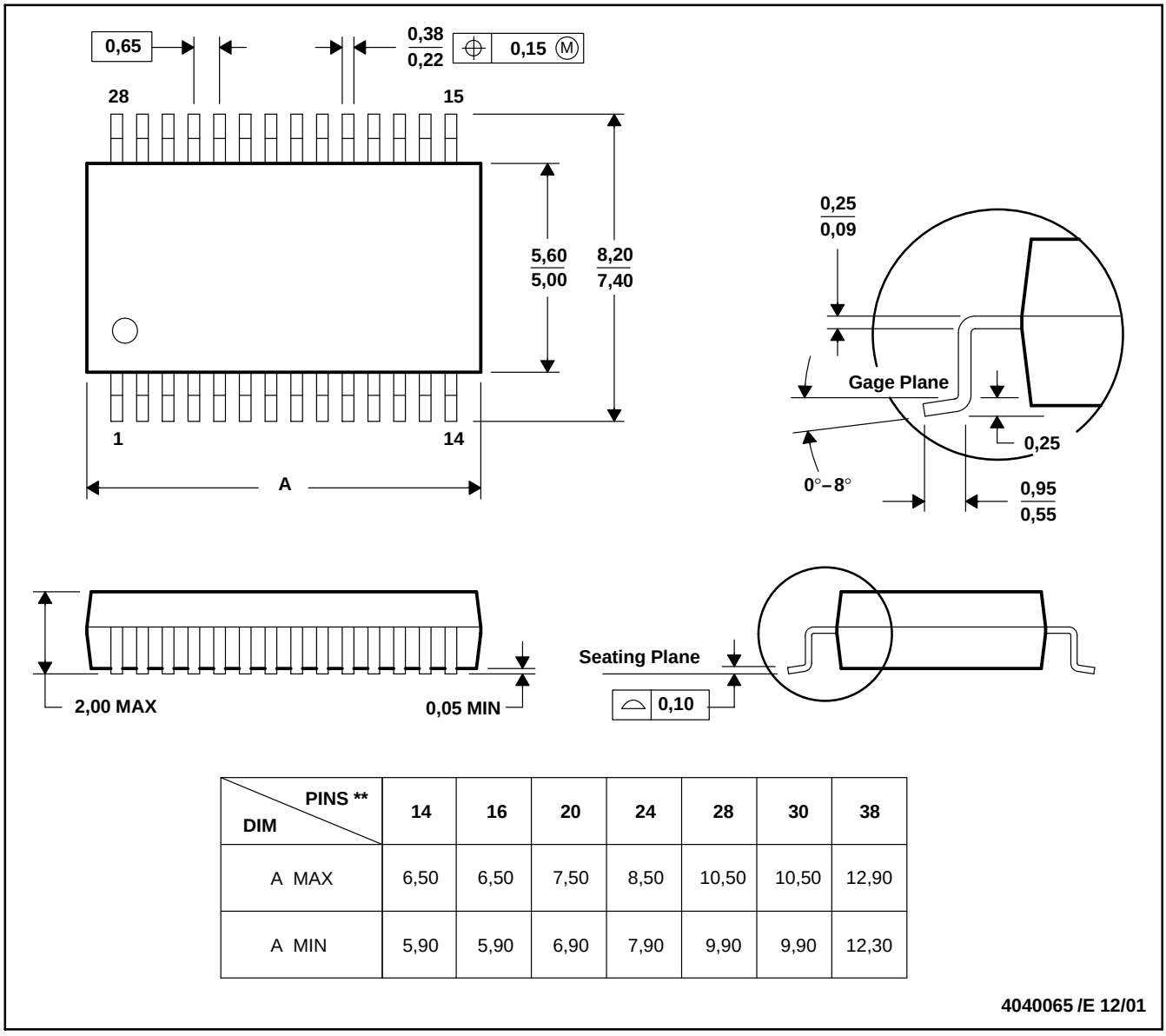
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS00DBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74LS00DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LS00NSR	SO	NS	14	2000	346.0	346.0	33.0
SN74LS00PSR	SO	PS	8	2000	346.0	346.0	33.0
SN74S00DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74S00NSR	SO	NS	14	2000	346.0	346.0	33.0

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



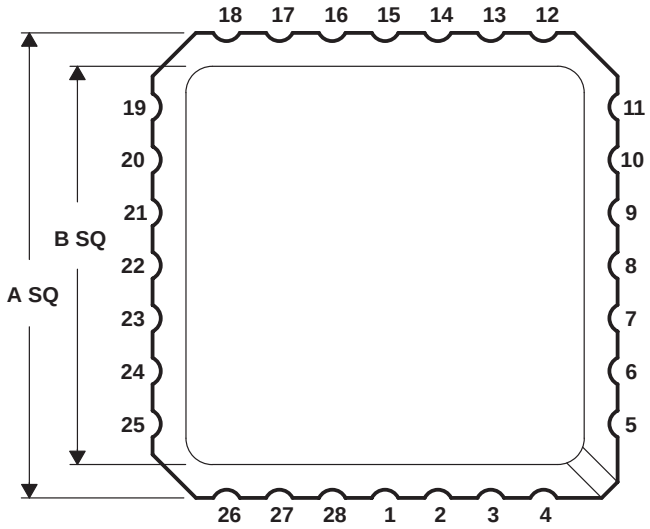
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

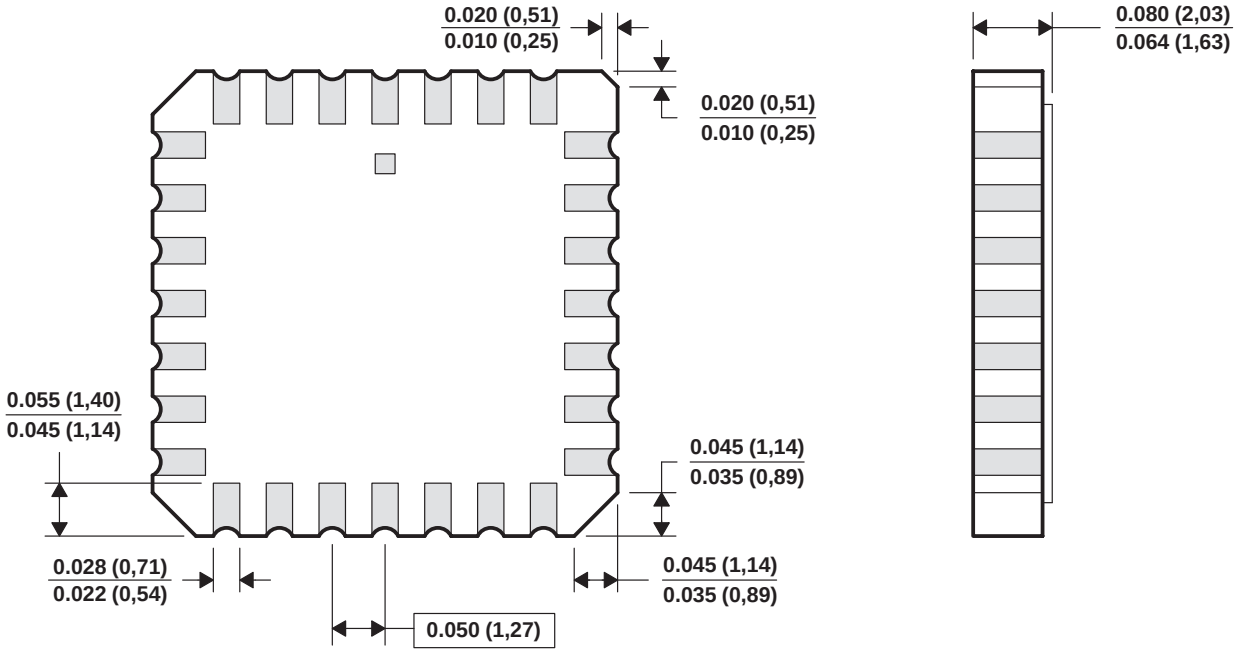
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



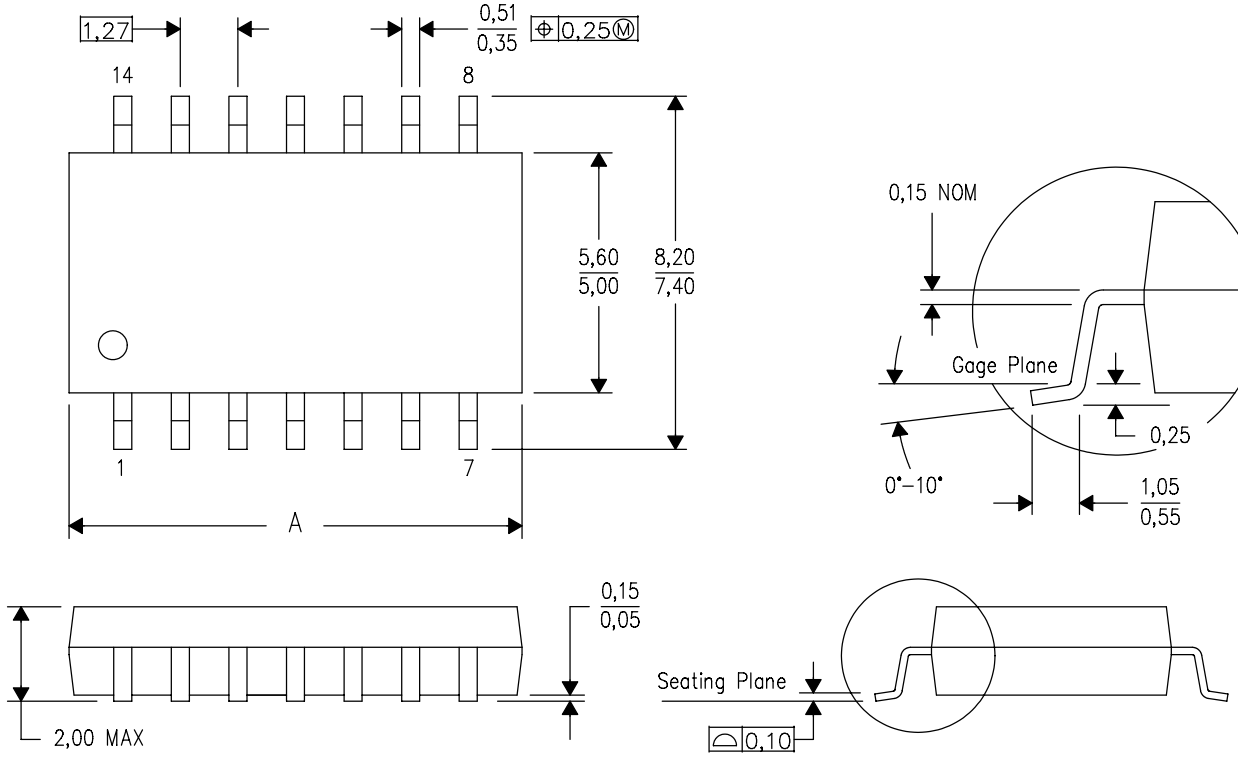
4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

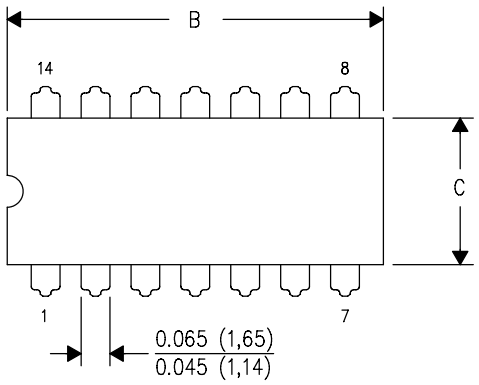
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

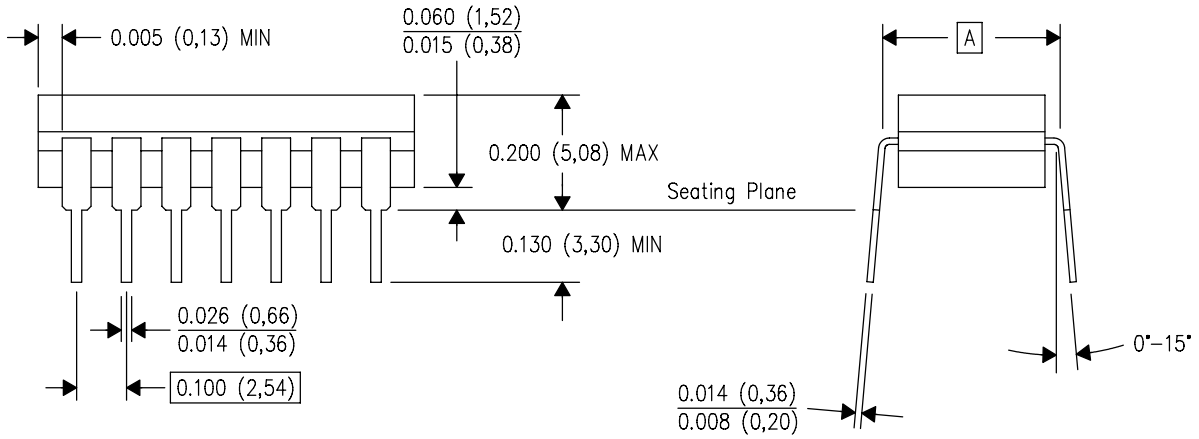
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

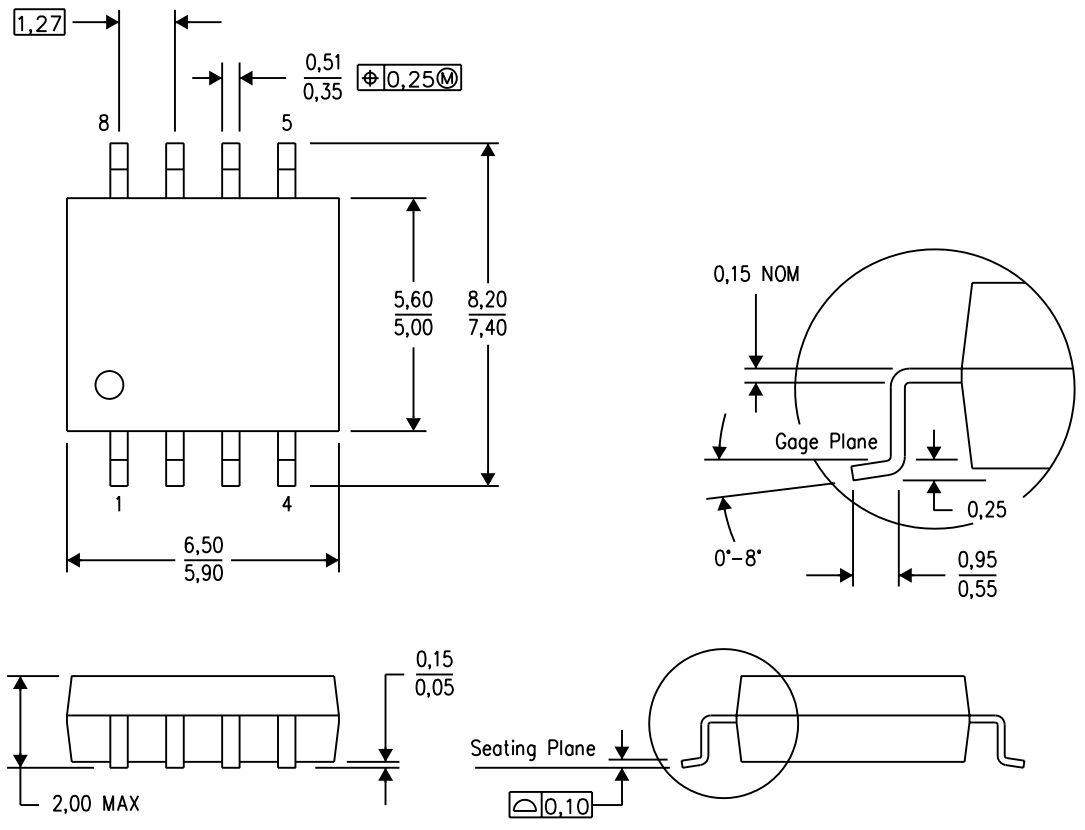


4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MECHANICAL DATA

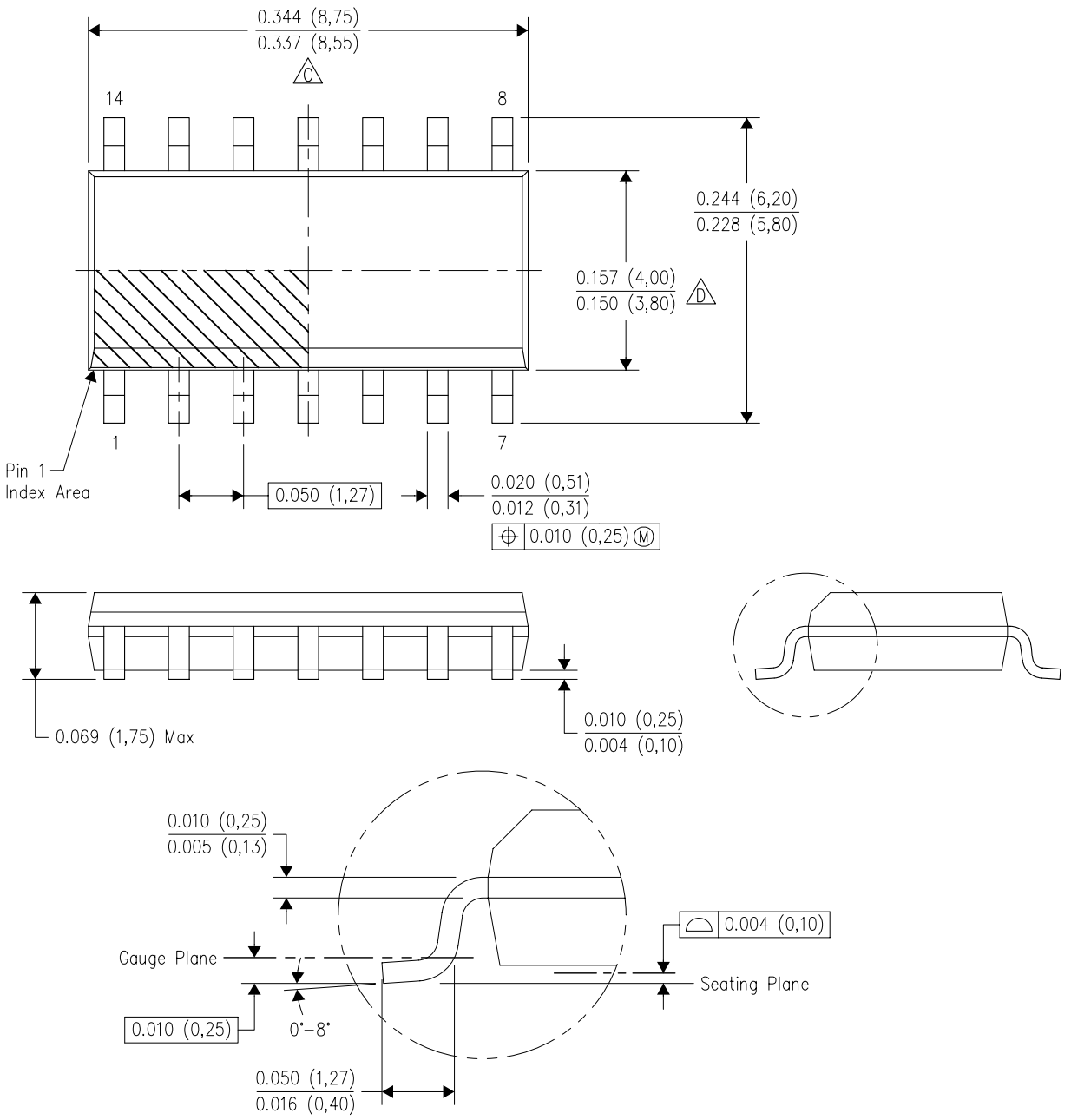
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

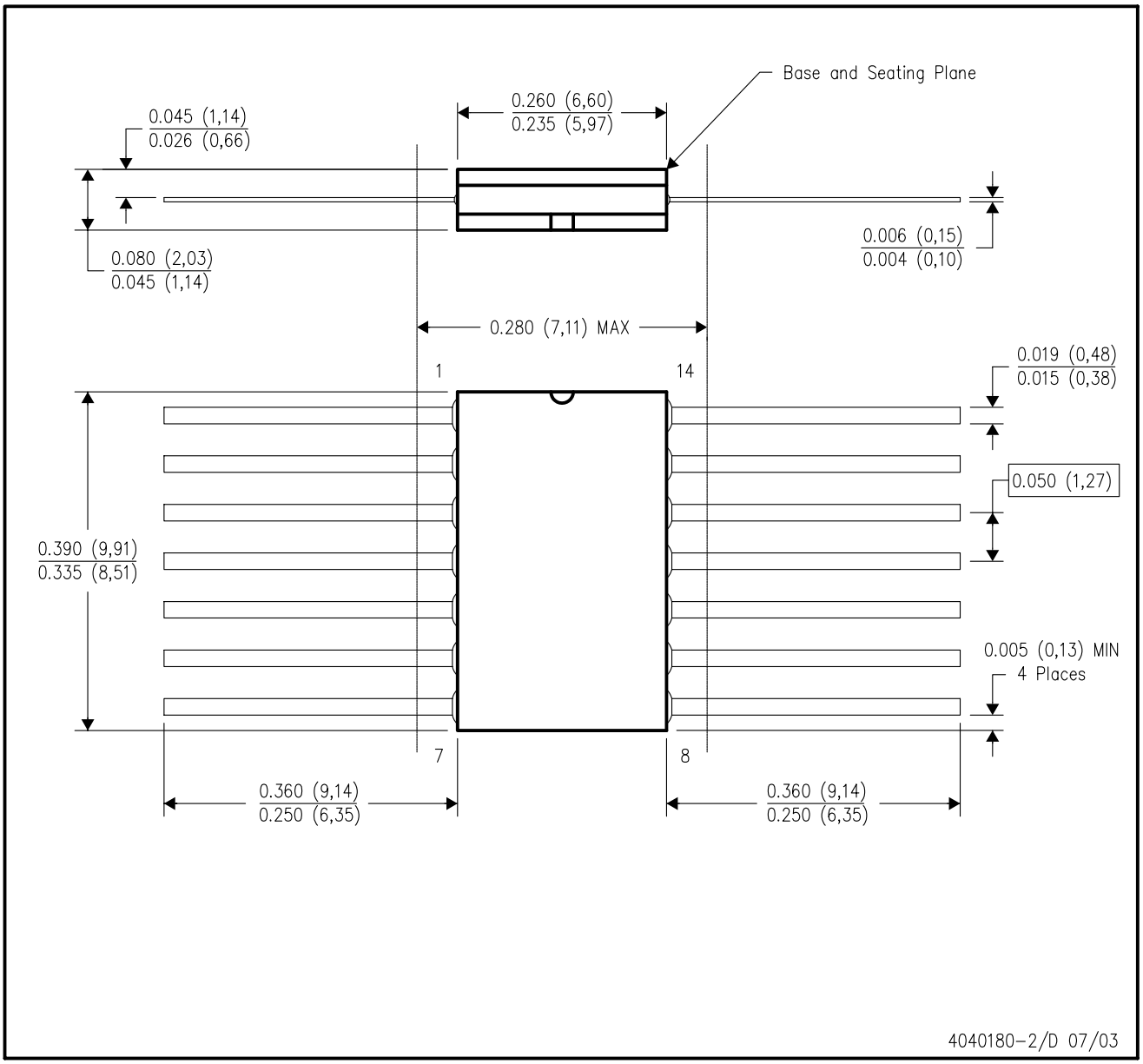
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

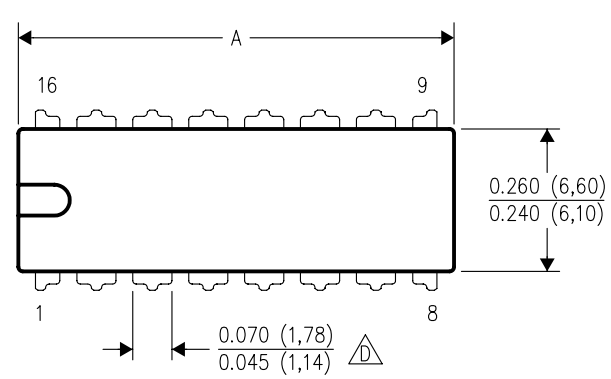


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

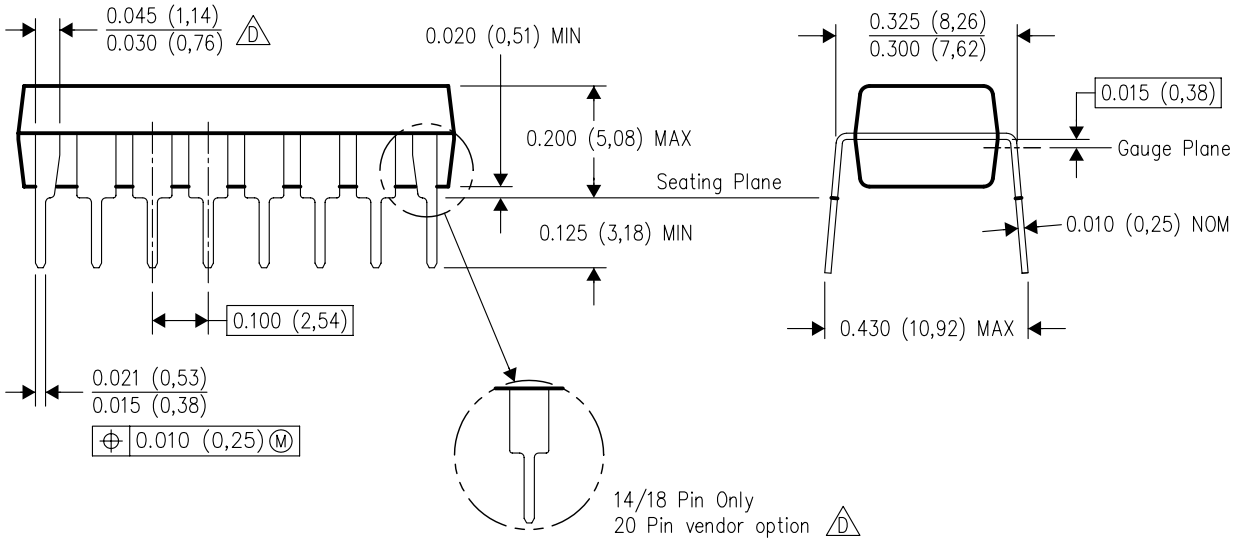
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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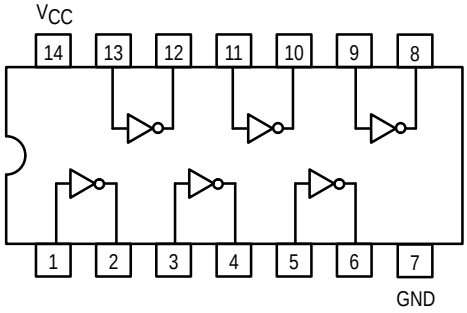
MOTOROLA

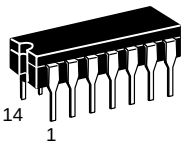
HEX INVERTER

SN54/74LS04

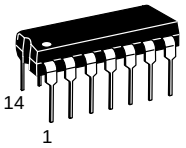


HEX INVERTER

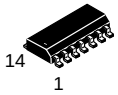
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			–0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				2.4	mA	V_{CC} = MAX	
	Total, Output LOW				6.6			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PLH}	Turn-Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn-On Delay, Input to Output		10	15	ns	

FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

CD4001BC/CD4011BC
Quad 2-Input NOR Buffered B Series Gate • Quad 2-Input NAND Buffered B Series Gate

General Description

The CD4001BC and CD4011BC quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Low power TTL:
  Fan out of 2 driving 74L compatibility: or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

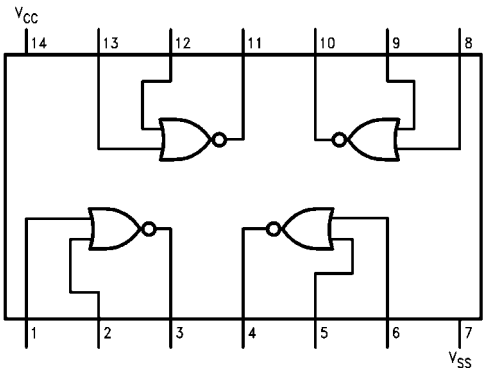
Ordering Code:

Order Number	Package Number	Package Description
CD4001BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150” Narrow
CD4001BCSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4001BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
CD4011BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150” Narrow
CD4011BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

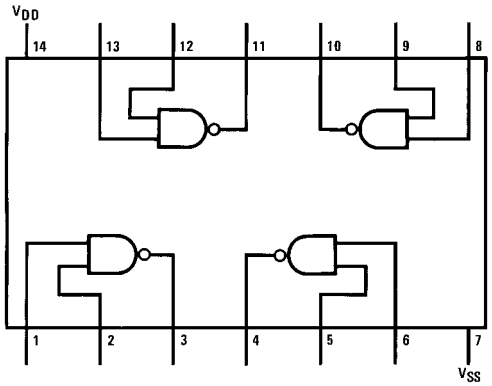
Connection Diagrams

Pin Assignments for DIP, SOIC and SOP
CD4001BC



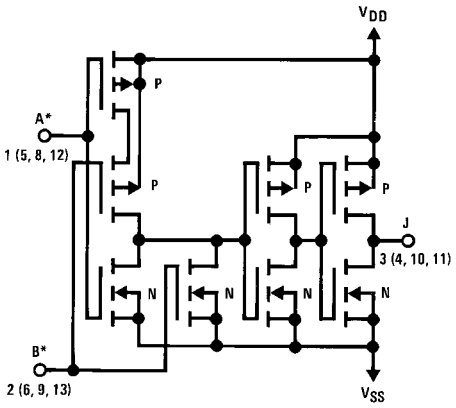
Top View

Pin Assignments for DIP and SOIC
CD4011BC

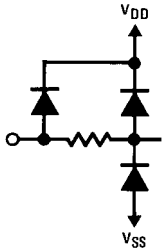


Top View

Schematic Diagrams



CD4001BC



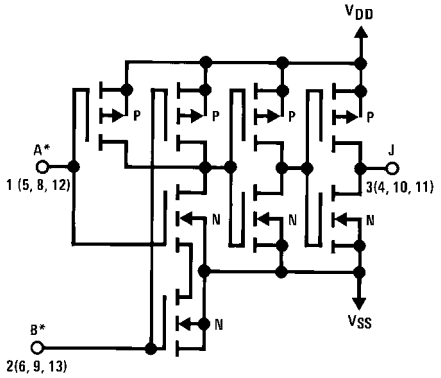
1/4 of device shown

$J = \overline{A + B}$

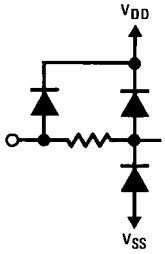
Logical "1" = HIGH

Logical "0" = LOW

All inputs protected by standard CMOS protection circuit.



CD4011BC



1/4 of device shown

$J = \overline{A \cdot B}$

Logical "1" = HIGH

Logical "0" = LOW

All inputs protected by standard CMOS protection circuit.

Absolute Maximum Ratings(Note 1)

(Note 2)

Voltage at any Pin	−0.5V to V_{DD} +0.5V
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
V_{DD} Range	−0.5 V_{DC} to +18 V_{DC}
Storage Temperature (T_S)	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions

Operating Range (V_{DD})	3 V_{DC} to 15 V_{DC}
Operating Temperature Range	
CD4001BC, CD4011BC	−40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics tables provide conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1		0.004	1		7.5	µA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2		0.005	2		15	µA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4		0.006	4		30	µA
V_{OL}	LOW Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V $\lvert I_O \rvert$ < 1 µA		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V $\lvert I_O \rvert$ < 1 µA	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	V_{DD} = 5V, V_O = 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0		6	4.0		4.0	V
V_{IH}	HIGH Level Input Voltage	V_{DD} = 5V, V_O = 0.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0	9		11.0		V
I_{OL}	LOW Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	µA

Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics (Note 4)

CD4001BC: T_A = 25°C, Input t_r; t_f = 20 ns. C_L = 50 pF, R_L = 200k. Typical temperature coefficient is 0.3%/°C.

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level	V_{DD} = 5V	110	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics (Note 5)

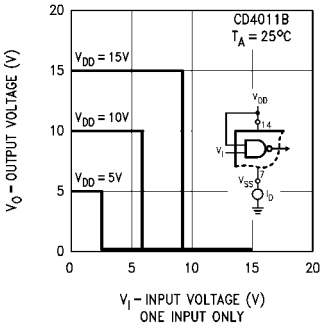
CD4011BC: $T_A = 25°C$, Input t_r; $t_f = 20$ ns. $C_L = 50$ pF, $R_L = 200$k. Typical Temperature Coefficient is 0.3%/°C.

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay,	$V_{DD} = 5V$	120	250	ns
	HIGH-to-LOW Level	$V_{DD} = 10V$	50	100	ns
		$V_{DD} = 15V$	35	70	ns
t_{PLH}	Propagation Delay,	$V_{DD} = 5V$	85	250	ns
	LOW-to-HIGH Level	$V_{DD} = 10V$	40	100	ns
		$V_{DD} = 15V$	30	70	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$	90	200	ns
		$V_{DD} = 10V$	50	100	ns
		$V_{DD} = 15V$	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

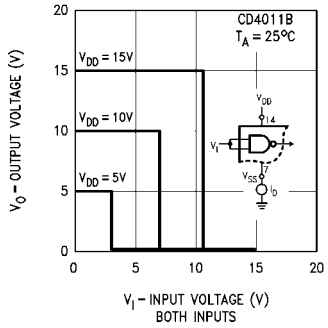
Note 5: AC Parameters are guaranteed by DC correlated testing.

Typical Performance Characteristics

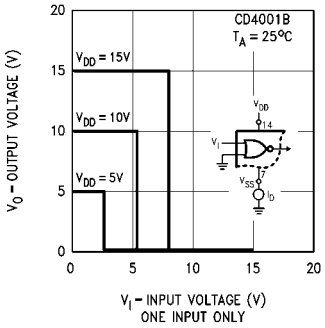
Typical Transfer Characteristics



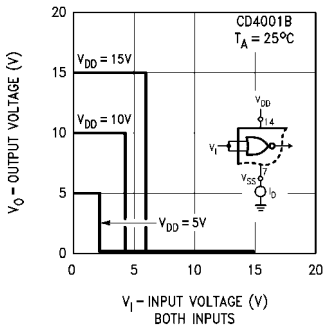
Typical Transfer Characteristics

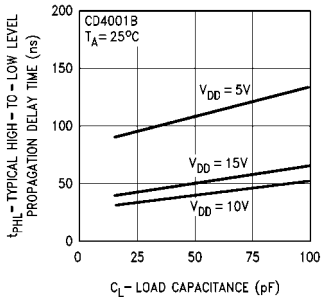


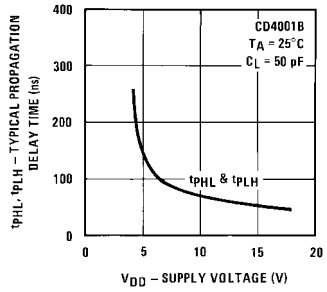
Typical Transfer Characteristics

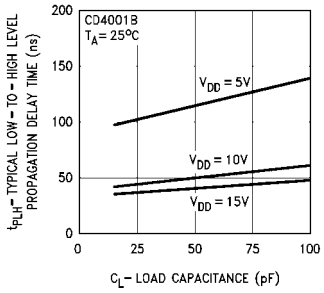


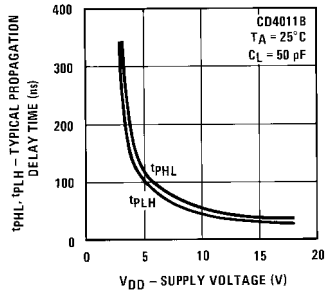
Typical Transfer Characteristics

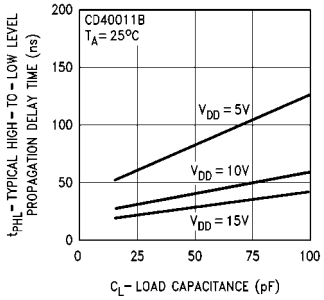


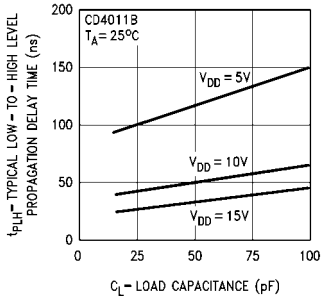


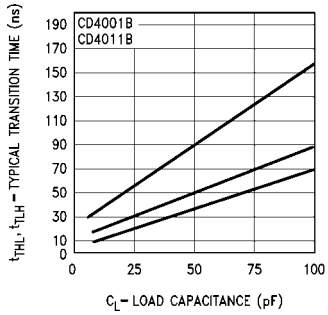


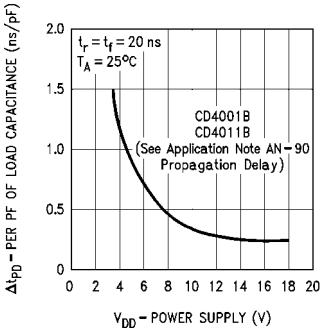


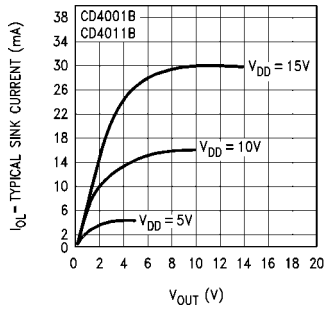


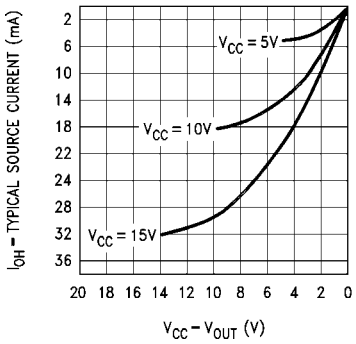



CD4011B
T_A = 25°C
V_{DD} = 5V
V_{DD} = 10V
V_{DD} = 15V
t_{PLH} – TYPICAL LOW – TO – HIGH LEVEL PROPAGATION DELAY TIME (ns)
C_L – LOAD CAPACITANCE (pF)

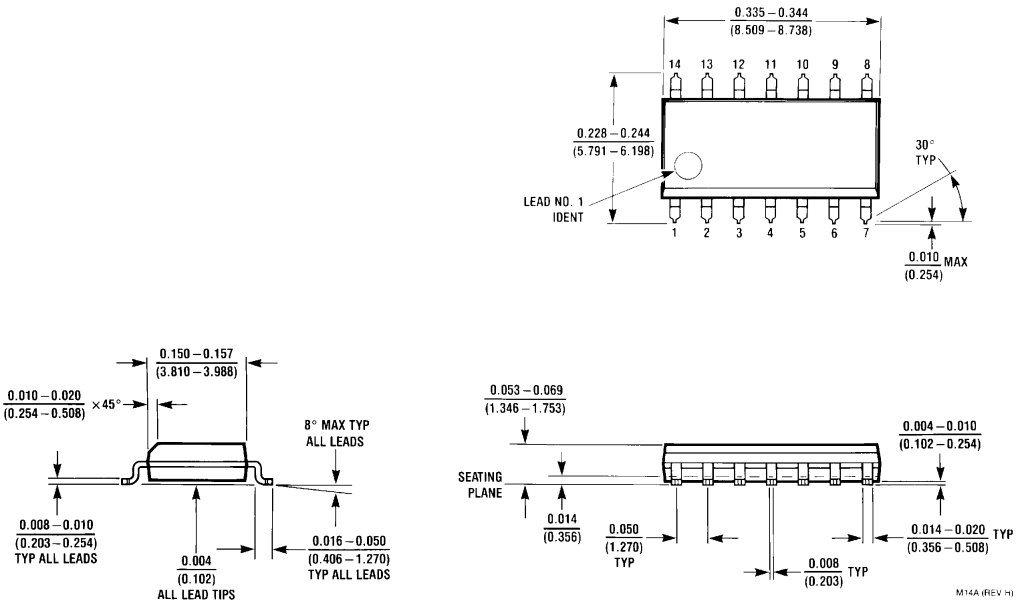

CD4001B
CD4011B
t_{THL}, t_{TLH} – TYPICAL TRANSITION TIME (ns)
C_L – LOAD CAPACITANCE (pF)


$t_r = t_f$ = 20 ns
T_A = 25°C
CD4001B
CD4011B
(See Application Note AN – 90
Propagation Delay)
Δt_{PD} – PER PF OF LOAD CAPACITANCE (ns/pF)
V_{DD} – POWER SUPPLY (V)

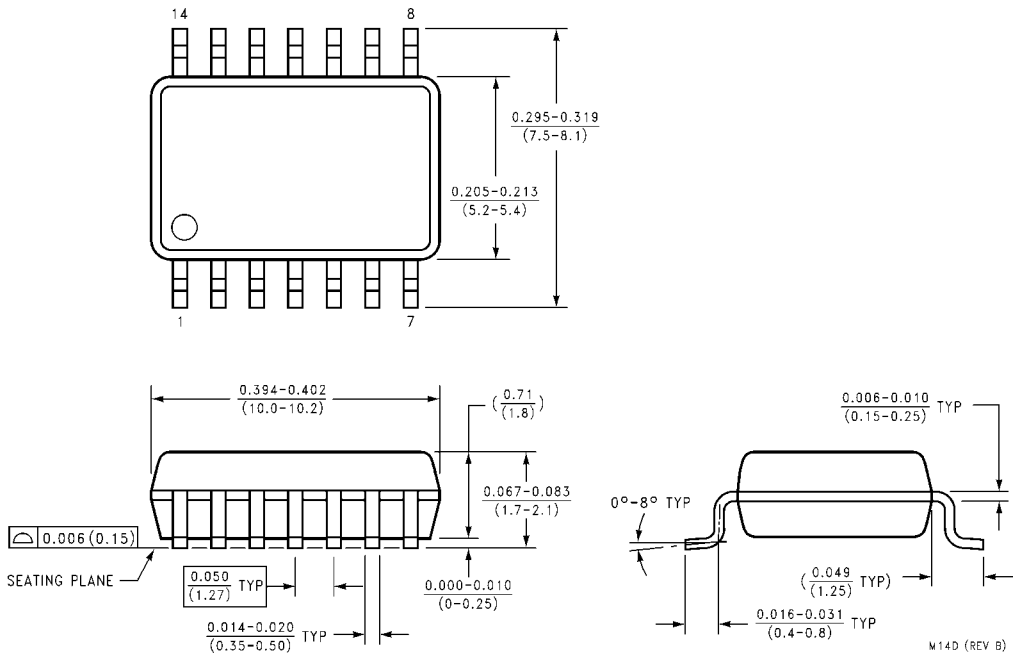

CD4001B
CD4011B
V_{DD} = 15V
V_{DD} = 10V
V_{DD} = 5V
I_{OL} – TYPICAL SINK CURRENT (mA)
V_{OUT} (V)


V_{CC} = 5V
V_{CC} = 10V
V_{CC} = 15V
I_{OH} – TYPICAL SOURCE CURRENT (mA)
$V_{CC} – V_{OUT}$ (V)

Physical Dimensions inches (millimeters) unless otherwise noted

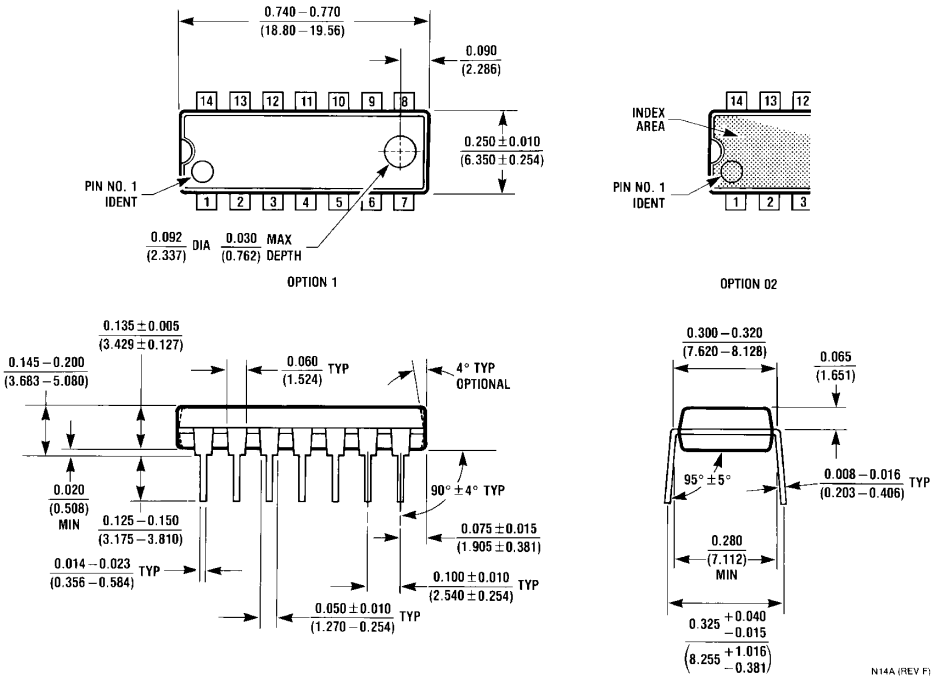


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
Package Number M14A



14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT14
Hex inverting Schmitt trigger

Product specification
File under Integrated Circuits, IC06

September 1993

Philips
Semiconductors

PHILIPS

Hex inverting Schmitt trigger 74HC/HCT14

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT14 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT14 provide six inverting buffers with Schmitt-trigger action. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	12	17	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	7	8	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

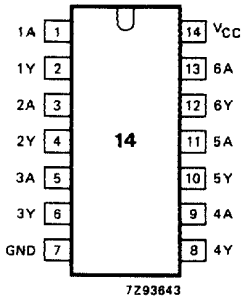


Fig.1 Pin configuration.

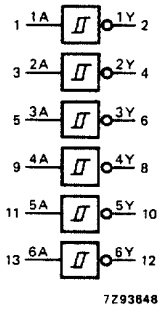


Fig.2 Logic symbol.

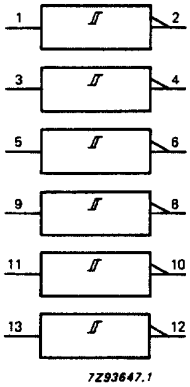


Fig.3 IEC logic symbol.

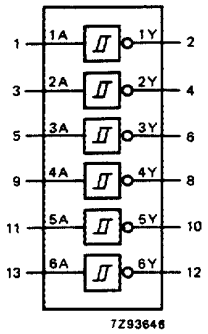


Fig.4 Functional diagram.

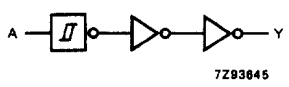


Fig.5 Logic diagram (one Schmitt trigger).

FUNCTION TABLE

INPUT	OUTPUT
nA	**nY**
L	H
H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level

APPLICATIONS

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*. Transfer characteristics are given below.

Output capability: standard
I_{CC} category: SSI

Transfer characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_T+	positive-going threshold	0.7 1.7 2.1	1.18 2.38 3.14	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	V	2.0 4.5 6.0	Figs 6 and 7
V_T–	negative-going threshold	0.3 0.9 1.2	0.52 1.40 1.89	0.90 2.00 2.60	0.3 0.90 1.20	0.90 2.00 2.60	0.30 0.90 1.2	0.90 2.00 2.60	V	2.0 4.5 6.0	Figs 6 and 7
V_H	hysteresis (V_T+ – V_T–)	0.2 0.4 0.6	0.66 0.98 1.25	1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	V	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_f = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.8
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 15		110 22 19	ns	2.0 4.5 6.0	Fig.8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*. Transfer characteristics are given below.

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA	0.3

Transfer characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_T+	positive-going threshold	1.2 1.4	1.41 1.59	1.9 2.1	1.2 1.4	1.9 2.1	1.2 1.4	1.9 2.1	V	4.5 5.5	Figs 6 and 7
V_T–	negative-going threshold	0.5 0.6	0.85 0.99	1.2 1.4	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	V	4.5 5.5	Figs 6 and 7
V_H	hysteresis (V_T+ –V_T–)	0.4 0.4	0.56 0.60	– –	0.4 0.4	– –	0.4 0.4	– –	V	4.5 5.5	Figs 6 and 7

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, to nY		20	34		43		51	ns	4.5	Fig.8
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.8

TRANSFER CHARACTERISTIC WAVEFORMS

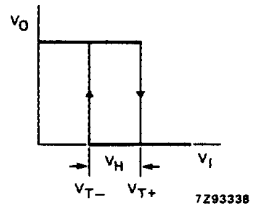


Fig.6 Transfer characteristic.

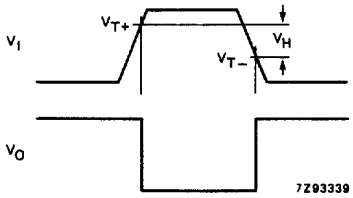


Fig.7 Waveforms showing the definition of V_T+, V_T- and V_H; where V_T+ and V_T- are between limits of 20% and 70%.

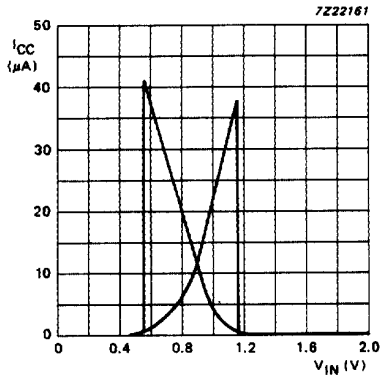


Fig.8 Typical HC transfer characteristics; V_{CC} = 2 V.

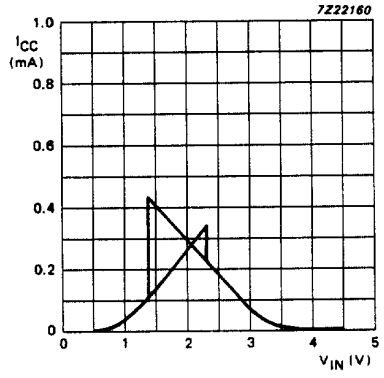


Fig.9 Typical HC transfer characteristics; V_{CC} = 4.5 V.

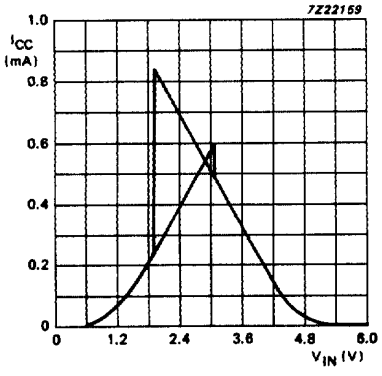


Fig.10 Typical HC transfer characteristics; V_{CC} = 6 V.

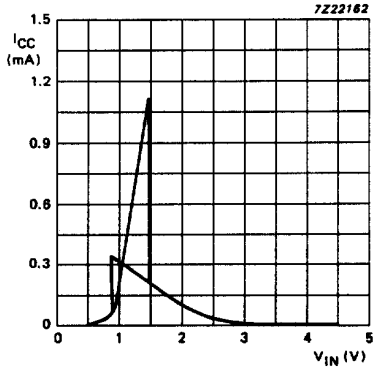


Fig.11 Typical HCT transfer characteristics; V_{CC} = 4.5 V.

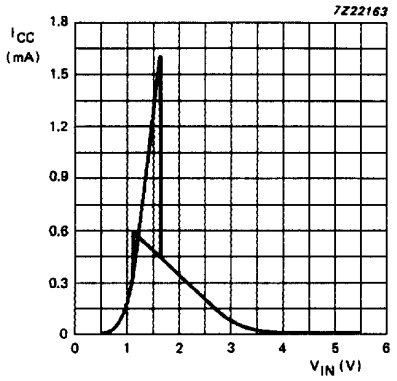
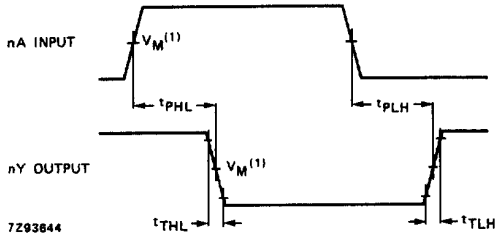


Fig.12 Typical HCT transfer characteristics; V_{CC} = 5.5 V.

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.13 Waveforms showing the input (nA) to output (nY) propagation delays and output transitions times.

APPLICATION INFORMATION

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{ad} = f_i \times (t_r \times I_{CCa} + t_f \times I_{CCa}) \times V_{CC}$.

Where:

P_{ad}	= additional power dissipation (μW)
f_i	= input frequency (MHz)
t_r	= input rise time (μs); 10% – 90%
t_f	= input fall time (μs); 10% – 90%
I_{CCa}	= average additional supply current (μA)

Average I_{CCa} differs with positive or negative input transitions, as shown in Figs 14 and 15.

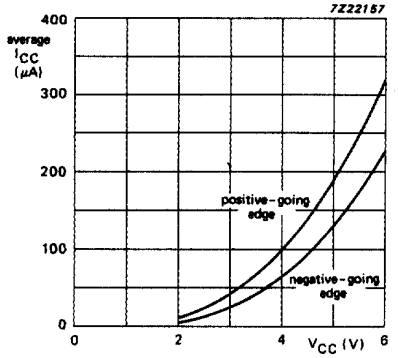


Fig.14 Average I_{CC} for HC Schmitt trigger devices; linear change of V_i between 0.1 V_{CC} to 0.9 V_{CC}

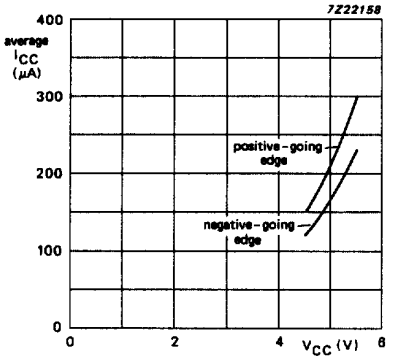


Fig.15 Average I_{CC} for HCT Schmitt trigger devices; linear change of V_i between 0.1 V_{CC} to 0.9 V_{CC}.

HC/HCT14 used in a relaxation oscillator circuit, see Fig.16.

HC : $f = \frac{1}{T} \approx \frac{1}{0.8\ RC}$

HCT : $f = \frac{1}{T} \approx \frac{1}{0.67\ RC}$

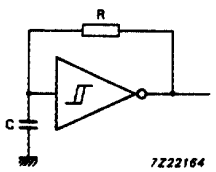


Fig.16 Relaxation oscillator using HC/HCT14.

Note to Application information

All values given are typical unless otherwise specified.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

National Semiconductor

July 2006

LM555 Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

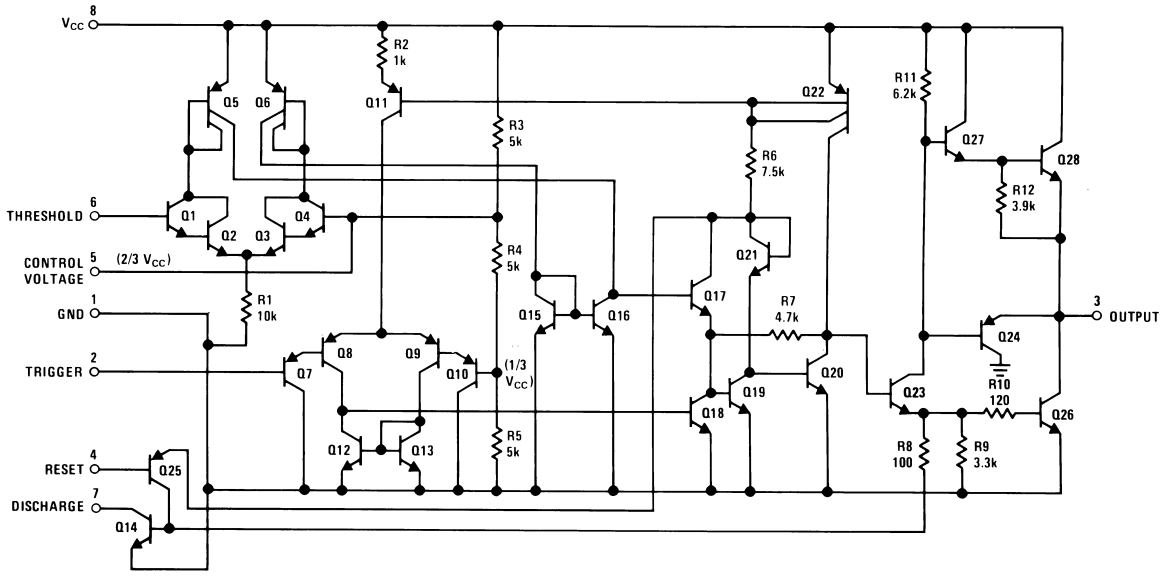
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per ˚C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



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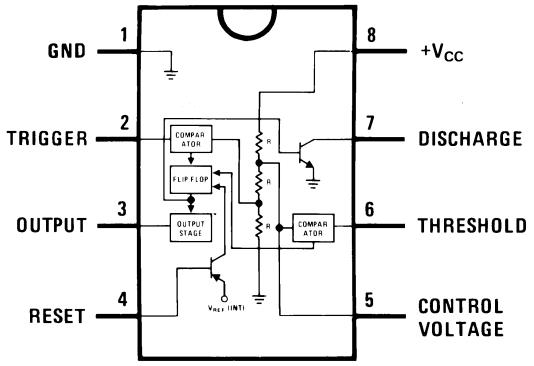
Connection Diagram

Dual-In-Line, Small Outline and Molded Mini Small Outline Packages



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Top View

Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555CM, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Soldering Information

Dual-In-Line Package	
Soldering (10 Seconds)	260˚C
Small Outline Packages	
(SOIC and MSOP)	
Vapor Phase (60 Seconds)	215˚C
Infrared (15 Seconds)	220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

(T_A = 25˚C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Supply Voltage		4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	6	
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 4)		10	15	mA
Timing Error, Monostable					
Initial Accuracy			1		%
Drift with Temperature	R_A = 1k to 100kΩ, C = 0.1µF, (Note 5)		50		ppm/˚C
Accuracy over Temperature			1.5		%
Drift with Supply			0.1		%/V
Timing Error, Astable					
Initial Accuracy			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100kΩ, C = 0.1µF, (Note 5)		150		ppm/˚C
Accuracy over Temperature			3.0		%
Drift with Supply			0.30		%/V
Threshold Voltage			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V		5		V
	V_{CC} = 5V		1.67		V
Trigger Current			0.5	0.9	µA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25	µA
Control Voltage Level	V_{CC} = 15V	9	10	11	V
	V_{CC} = 5V	2.6	3.33	4	
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat (Note 7)					
Output Low	V_{CC} = 15V, I_7 = 15mA		180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5mA		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25˚C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V				
	I_{SINK} = 10mA		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.75	V
	I_{SINK} = 100mA		2	2.5	V
	I_{SINK} = 200mA		2.5		V
	V_{CC} = 5V				
	I_{SINK} = 8mA				V
	I_{SINK} = 5mA		0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200mA, V_{CC} = 15V		12.5		V
	I_{SOURCE} = 100mA, V_{CC} = 15V	12.75	13.3		V
	V_{CC} = 5V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25˚C based on a +150˚C maximum junction temperature and a thermal resistance of 106˚C/W (DIP), 170˚C/W (S0-8), and 204˚C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

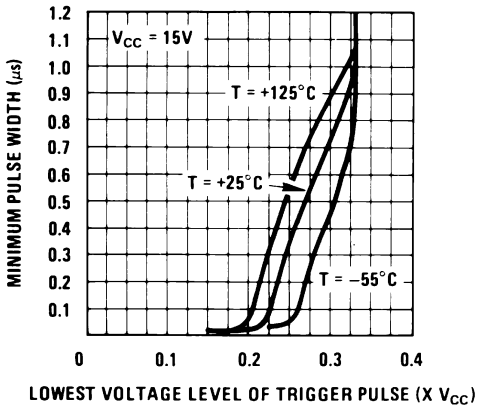
Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20MΩ.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Typical Performance Characteristics

Minimuim Pulse Width Required for Triggering



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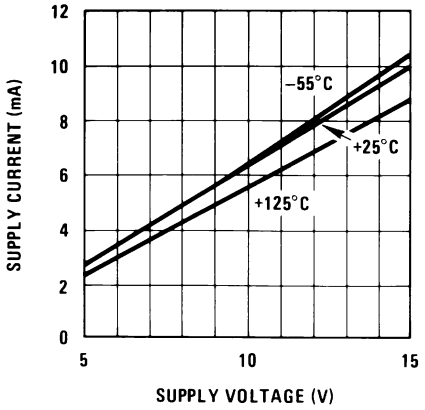
Supply Current vs. Supply Voltage



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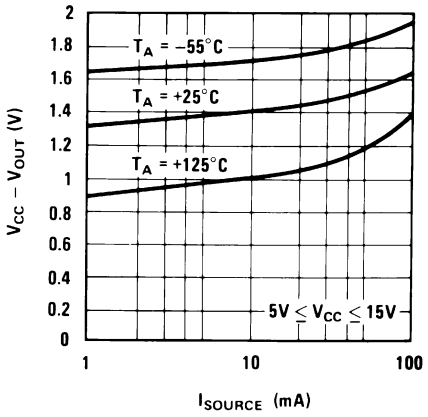
High Output Voltage vs. Output Source Current



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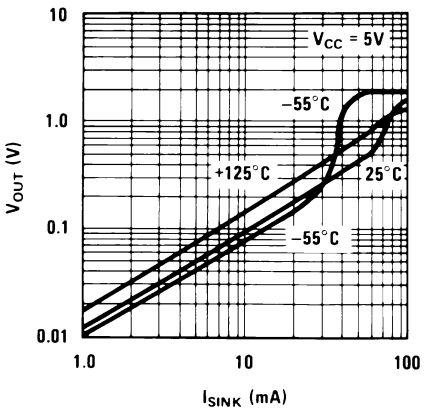
Low Output Voltage vs. Output Sink Current



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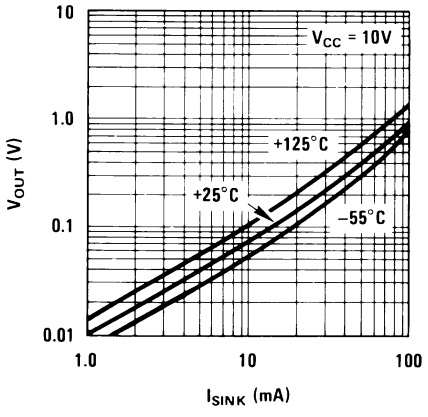
Low Output Voltage vs. Output Sink Current



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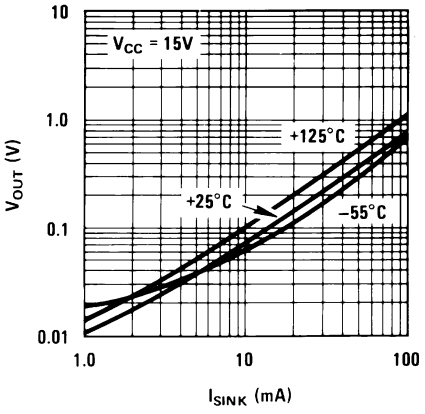
Low Output Voltage vs. Output Sink Current



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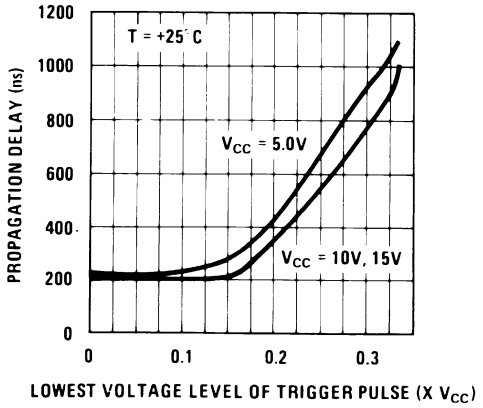
Typical Performance Characteristics (Continued)

Output Propagation Delay vs. Voltage Level of Trigger Pulse



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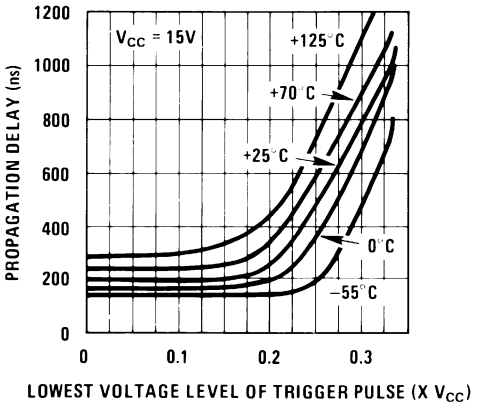
Output Propagation Delay vs. Voltage Level of Trigger Pulse



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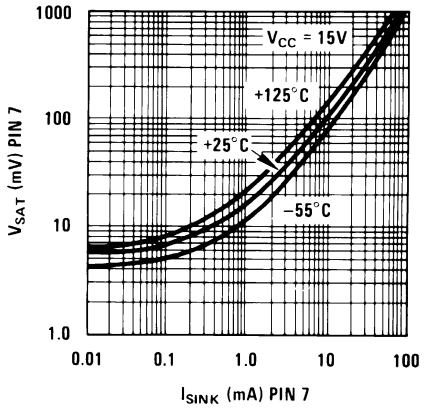
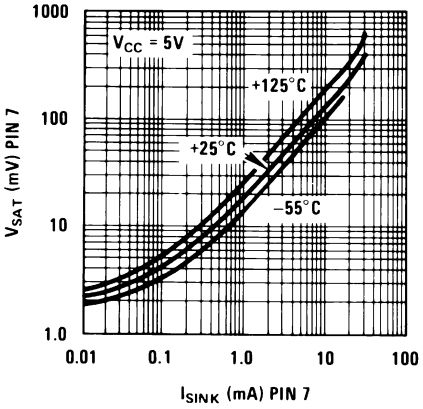
Discharge Transistor (Pin 7) Voltage vs. Sink Current



00785126

Discharge Transistor (Pin 7) Voltage vs. Sink Current



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Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

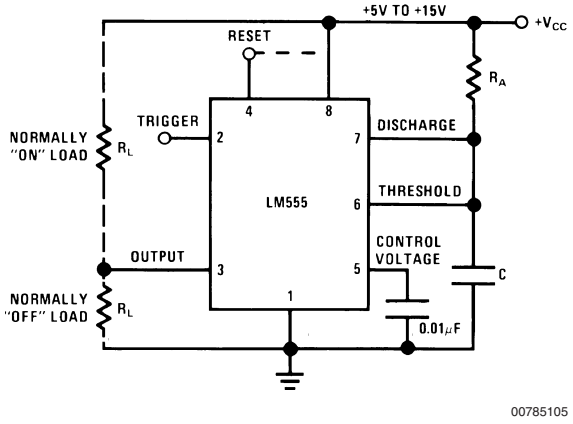
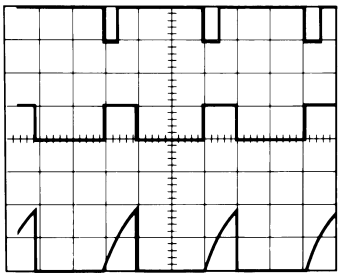


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



V_{CC} = 5V Top Trace: Input 5V/Div.
TIME = 0.1 ms/DIV. Middle Trace: Output 5V/Div.
R_A = 9.1kΩ Bottom Trace: Capacitor Voltage 2V/Div.
C = 0.01μF

FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

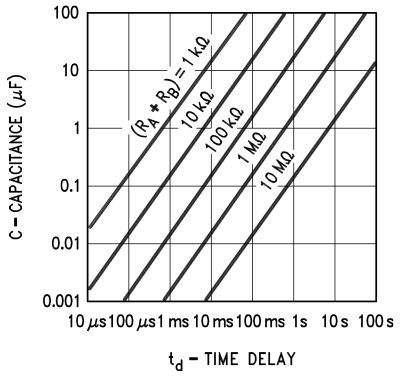


FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

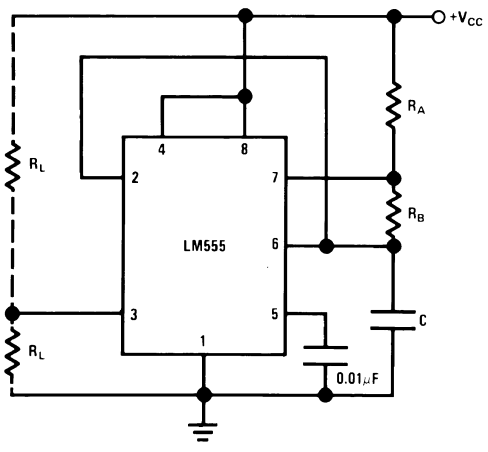
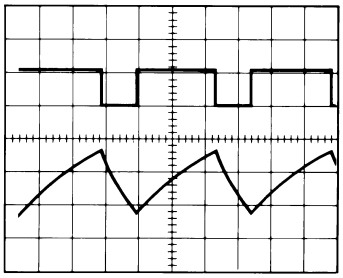


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



00785109

V_{CC} = 5V Top Trace: Output 5V/Div.
TIME = 20µs/DIV. Bottom Trace: Capacitor Voltage 1V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

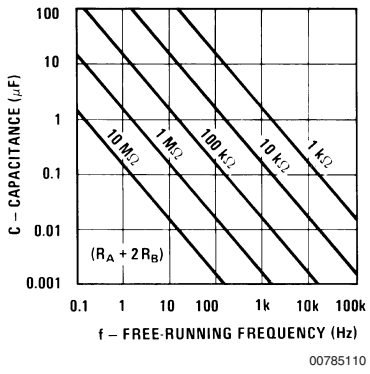


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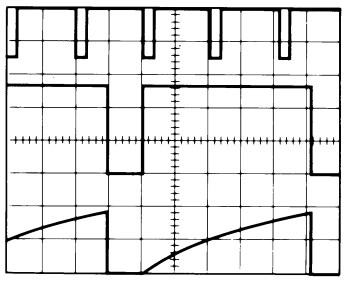
FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



00785111

V_{CC} = 5V Top Trace: Input 4V/Div.
TIME = 20µs/DIV. Middle Trace: Output 2V/Div.
R_A = 9.1kΩ Bottom Trace: Capacitor 2V/Div.
C = 0.01µF

FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

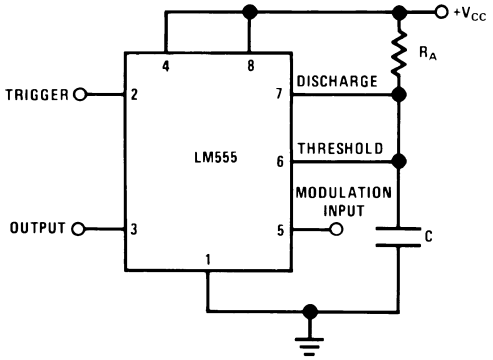


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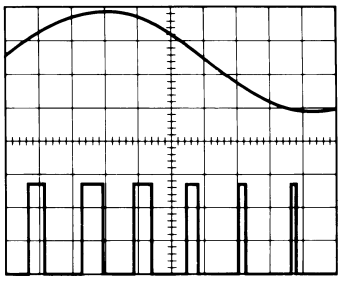
FIGURE 8. Pulse Width Modulator

Applications Information (Continued)



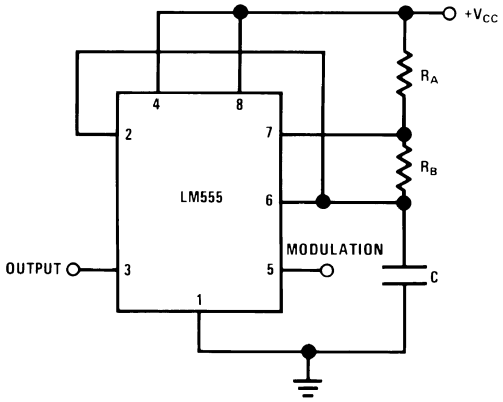
00785113

V_{CC} = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1kΩ
C = 0.01µF

FIGURE 9. Pulse Width Modulator

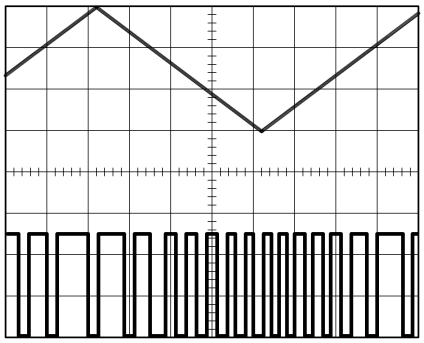
PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.



00785114

FIGURE 10. Pulse Position Modulator



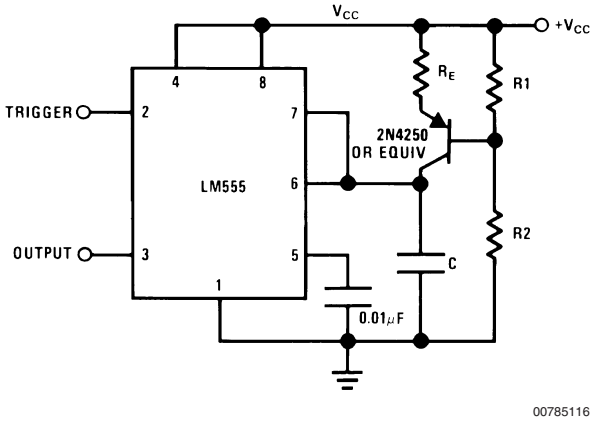
00785115

V_{CC} = 5V Top Trace: Modulation Input 1V/Div.
TIME = 0.1 ms/DIV. Bottom Trace: Output 2V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.



00785116

FIGURE 12.

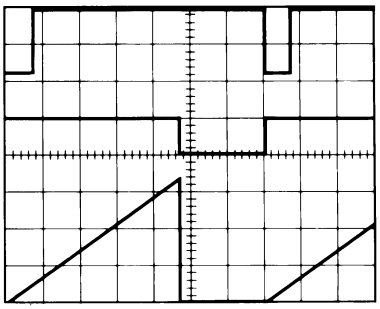
Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\ V_{CC}\ R_E\ (R_1 + R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$

$$V_{BE} \simeq 0.6V$$

Applications Information (Continued)



00785117

V_{CC} = 5V Top Trace: Input 3V/Div.
TIME = 20µs/DIV. Middle Trace: Output 5V/Div.
R_1 = 47kΩ Bottom Trace: Capacitor Voltage 1V/Div.
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 µF

FIGURE 13. Linear Ramp

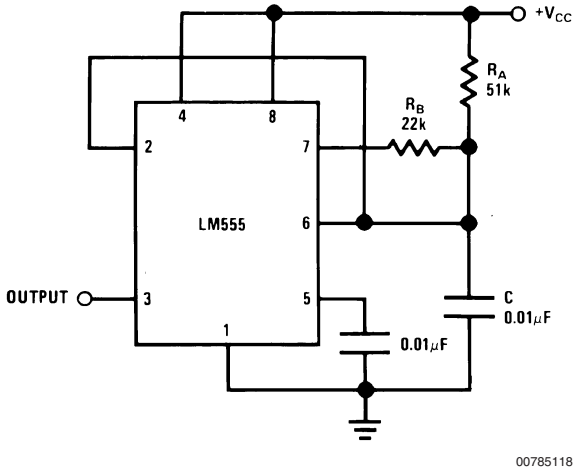
50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is t_2 =

$$\left[(R_A\ R_B)/(R_A + R_B)\right] C\ \ell n \left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$



00785118

FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

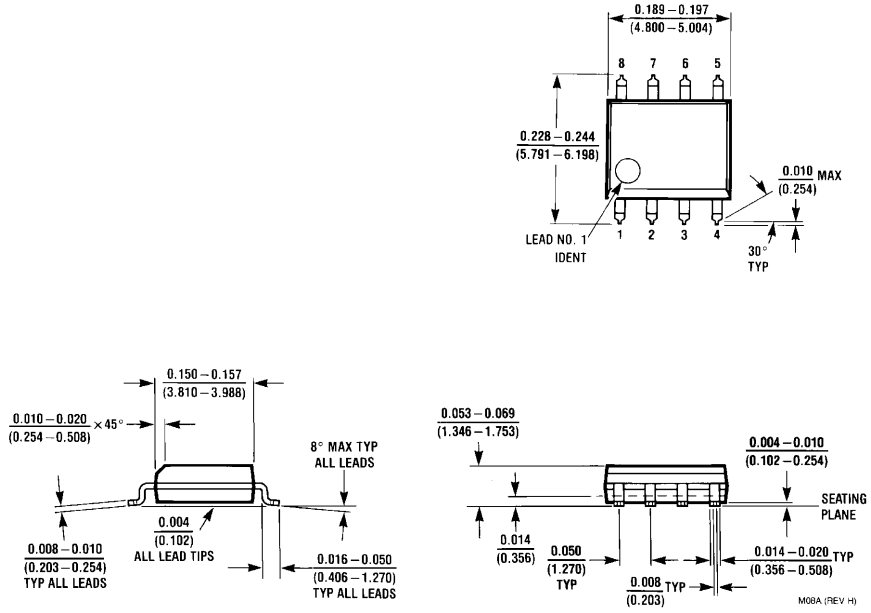
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

Lower comparator storage time can be as long as 10µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10µs minimum.

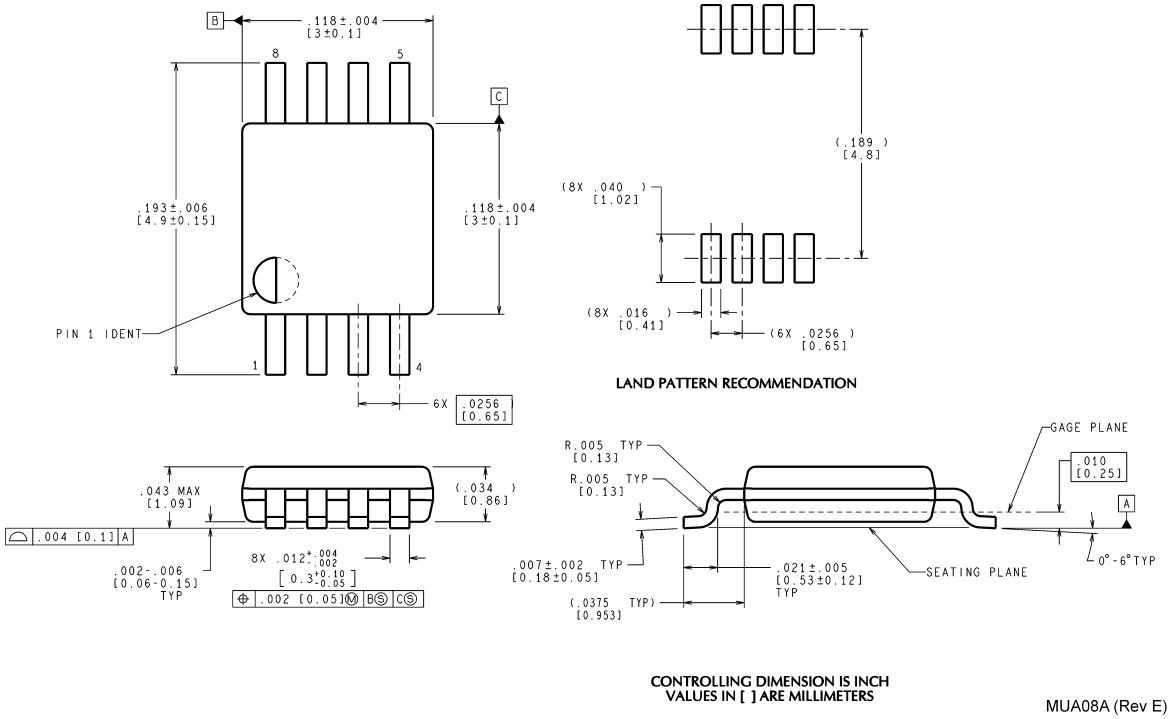
Delay time reset to output is 0.47µs typical. Minimum reset pulse width must be 0.3µs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

Physical Dimensions inches (millimeters) unless otherwise noted

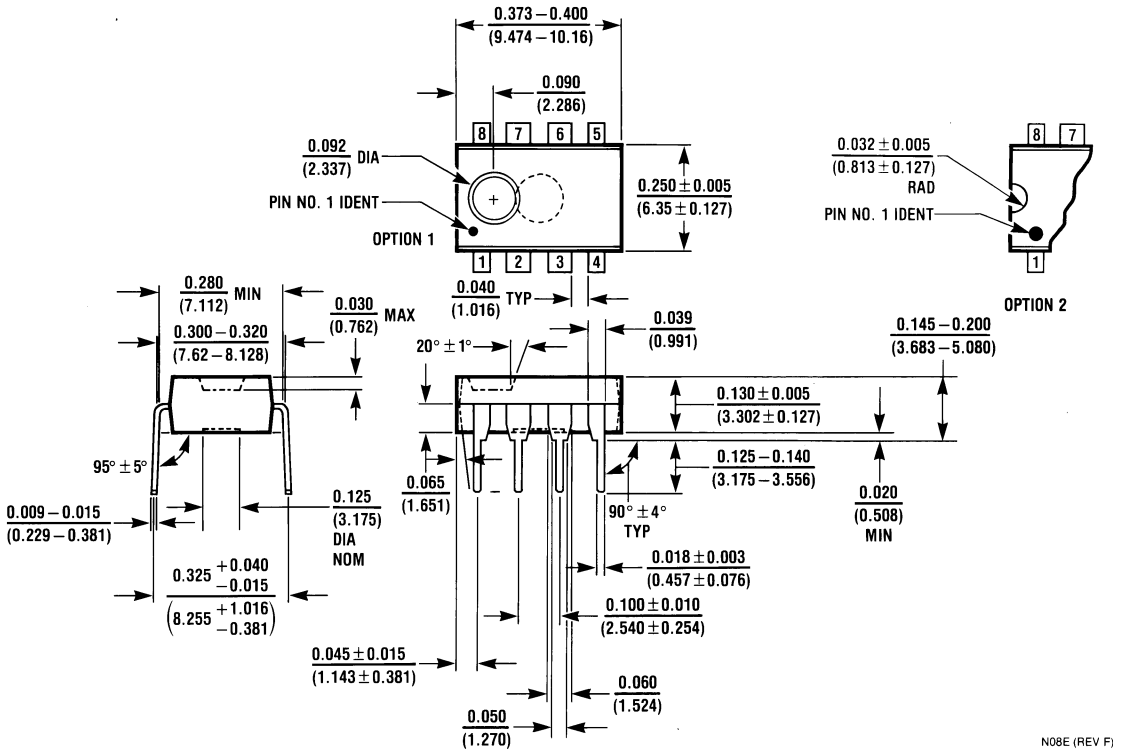


Small Outline Package (M)
NS Package Number M08A



8-Lead (0.118” Wide) Molded Mini Small Outline Package
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
NS Package Number N08E

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560

- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

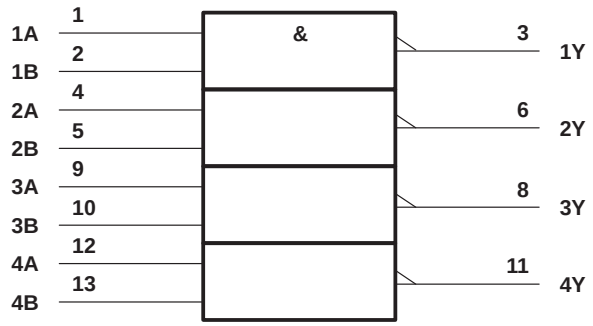
These devices contain four independent 2-input positive-NAND gates. They perform the Boolean functions $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS00A and SN54AS00 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS00A and SN74AS00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

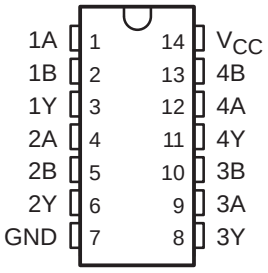
logic symbol†



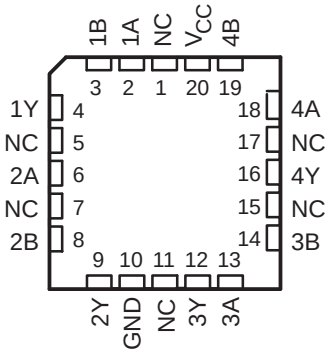
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

SN54ALS00A, SN54AS00 . . . J PACKAGE
SN74ALS00A, SN74AS00 . . . D OR N PACKAGE
(TOP VIEW)

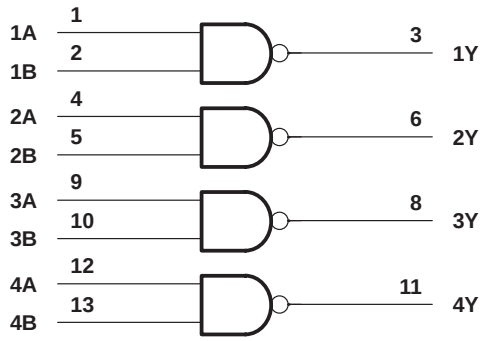


SN54ALS00A, SN54AS00 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A: SN54ALS00A . . . . . –55°C to 125°C
SN74ALS00A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS00A			SN74ALS00A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8‡			0.8	V
				0.7§				
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

‡ Applies over temperature range –55°C to 70°C
§ Applies over temperature range 70°C to 125°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS00A			SN74ALS00A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC} –2			V_{CC} –2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.1			–0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–20		–112	–30		–112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		0.5	0.85		0.5	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.5	3		1.5	3	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			SN54ALS00A		SN74ALS00A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	15	3	11	ns
t_{PHL}			2	9	2	8	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A: SN54AS00 . . . . . –55°C to 125°C
SN74AS00 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS00			SN74AS00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–2			–2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS00			SN74AS00			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC} –2			V_{CC} –2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5			–0.5	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		–112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		2	3.2		2	3.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		10.8	17.4		10.8	17.4	mA

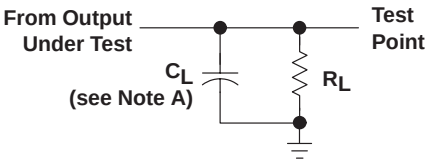
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

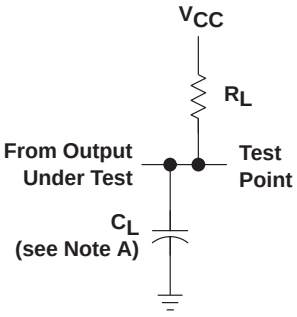
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			SN54AS00		SN74AS00		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4.5	ns
t_{PHL}			1	5	1	4	

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

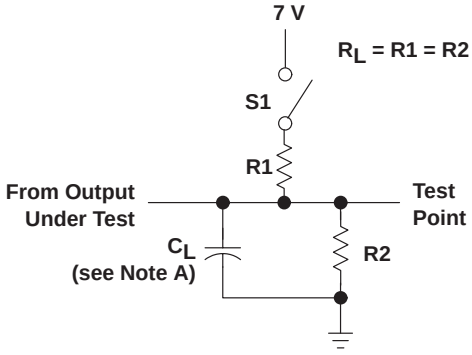
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



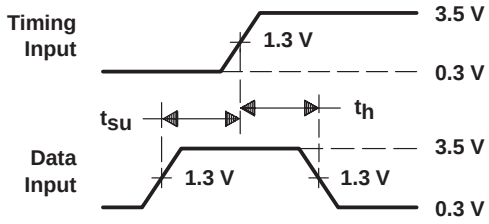
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



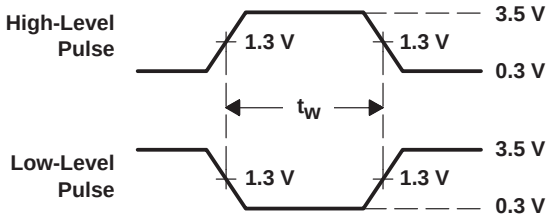
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



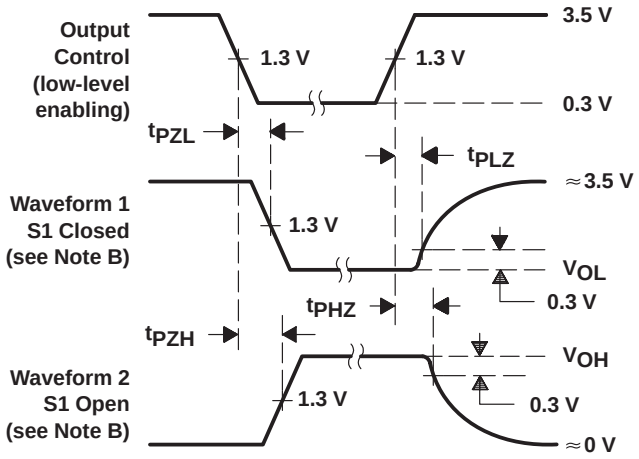
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



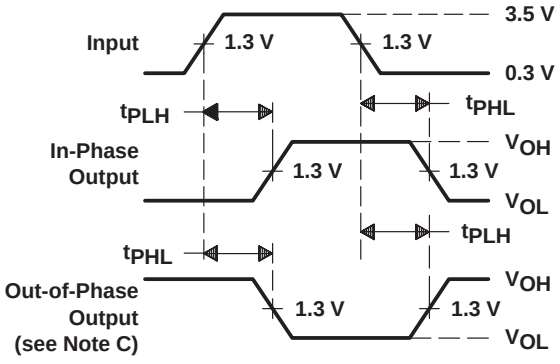
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS018C – Revised September 2003

CD4007UB Types

CMOS Dual Complementary Pair Plus Inverter

High-Voltage Types (20-Volt Rating)

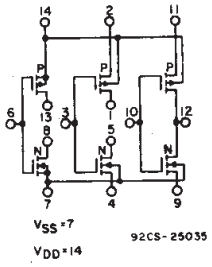
■ CD4007UB types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

The CD4007UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Standardized symmetrical output characteristics
- Medium Speed Operation – t_{PHL}, t_{PLH} = 30 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Meets all requirements of JEDEC Tentative **Standard No. 13B, "Standard Specifications** for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C



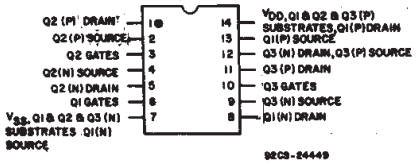
Terminal No.14 – V_{DD}
Terminal No. 7 – V_{SS}

FUNCTIONAL DIAGRAM

Applications:

- Extremely high-input impedance amplifiers
- Shapers
- Inverters
- Threshold detector
- Linear amplifiers
- Crystal oscillators

TERMINAL DIAGRAM
Top View



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

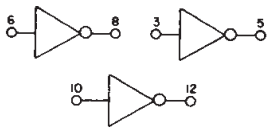
STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0;10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1				—	—	1	V
	9	–	10	2				—	—	2	
	13.5	–	15	2.5				—	—	2.5	
Input High Voltage, V_{IH} Min.	0.5	–	5	4				4	—	—	
	1	–	10	8				8	—	—	
	1.5	–	15	12.5				12.5	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

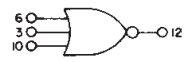
a) Triple Inverters



(14,2,11); (8,13);
(1,5); (7,4,9)

92CS-15350

b) 3-Input NOR Gate



92CS-15349

(13,2); (1,11);
(12,5,8); (7,4,9)

c) 3-Input NAND Gate

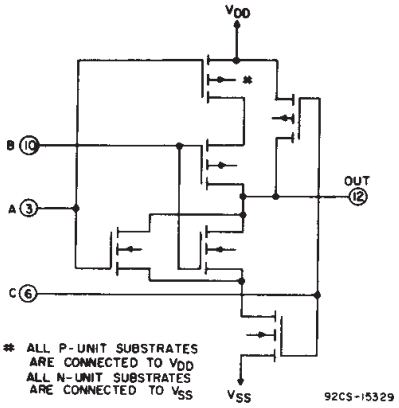
92CS-15348

(1,12,13); (2,14,11);
(4,8); (5,9)

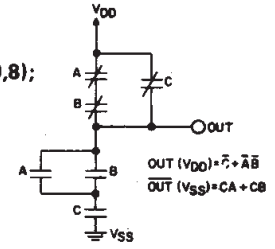
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS	LIMITS		UNITS
		V_{DD} Volts	Typ.	Max.	
Propagation Delay Time:	t_{PHL}, t_{PLH}	5	55	110	ns
		10	30	60	
		15	25	50	
Transition Time	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance	C_{IN}	Any Input	10	15	pF

d) Tree (Relay) Logic



92CS-15329



(13,12,5); (4,9,8);
(14,2); (1,11)

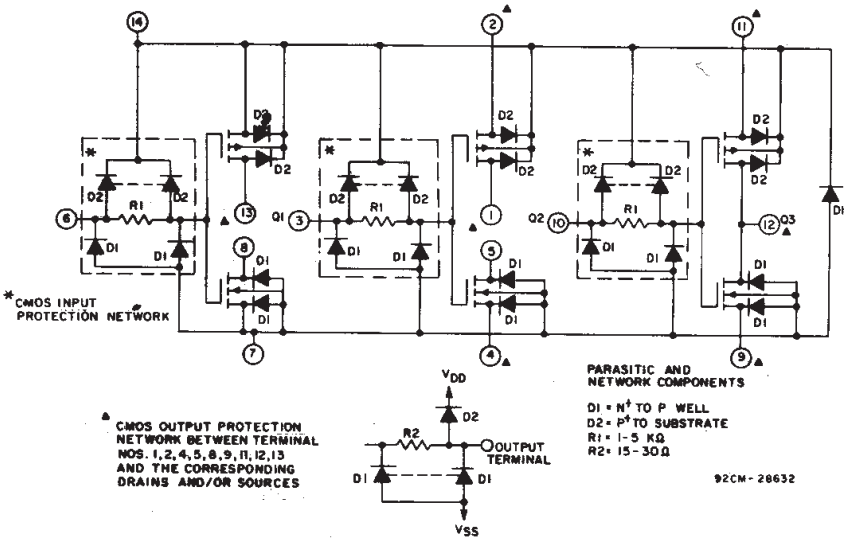
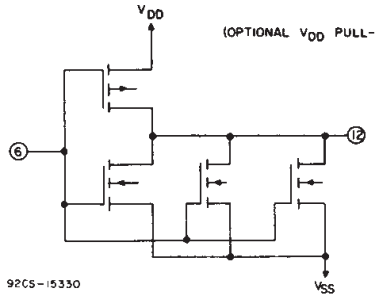


Fig. 1 – Detailed schematic diagram of CD4007UB showing input, output, and parasitic diodes.

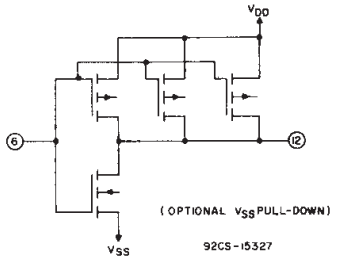
Fig. 2 – Sample CMOS logic circuit arrangements using type CD4007UB.

e) High Sink-Current Driver

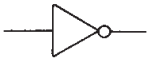


(6,3,10); (8.5, 12); (11,14); 7,4,9)

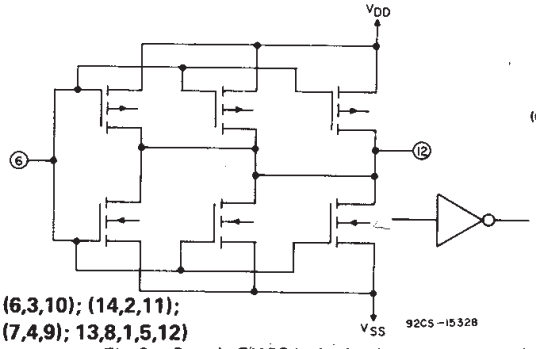
f) High Source-Current Driver



(6,3,10); (13,1,12); (14,2,11); (7,9)

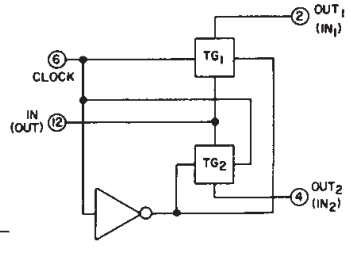


g) High Sink - and Source-Current Driver



(6,3,10); (14,2,11); (7,4,9); 13,8,1,5,12)

h) Dual Bi-Directional Transmission Gating



(1,5,12); (2,9); (11,4); (8,13,10); (6,3)

Fig. 2 – Sample CMOS logic circuit arrangements using type CD4007UB (Cont'd).

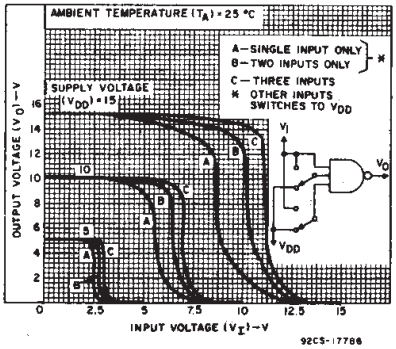


Fig. 3 – Typical voltage-transfer characteristics for NAND gate.

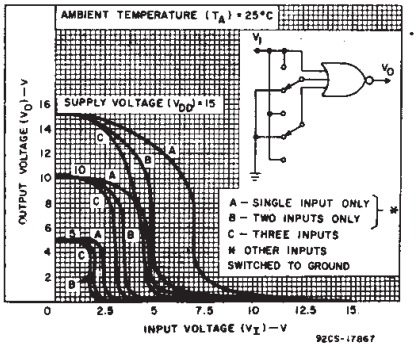


Fig. 4 – Typical voltage-transfer characteristics for NOR gate.

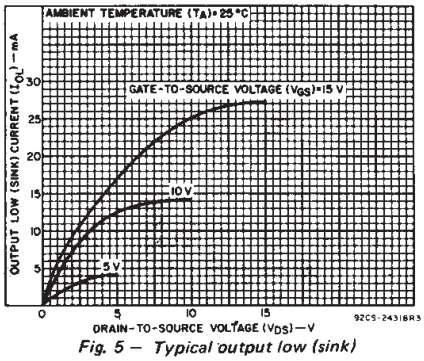


Fig. 5 – Typical output low (sink) current characteristics.

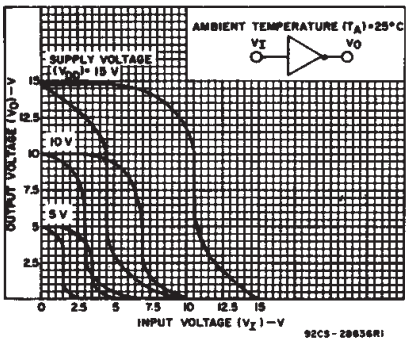


Fig. 6 – Minimum and maximum voltage-transfer characteristics for inverter.

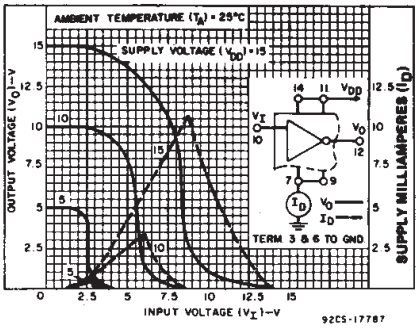


Fig. 7 – Typical current and voltage-transfer characteristics for inverter.

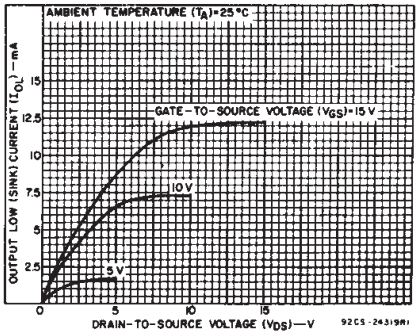


Fig. 8 – Minimum output low (sink) current characteristics.

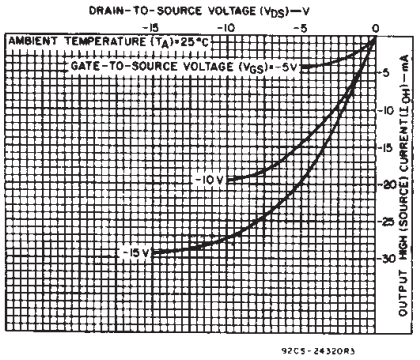


Fig. 9 – Typical output high (source) current characteristics.

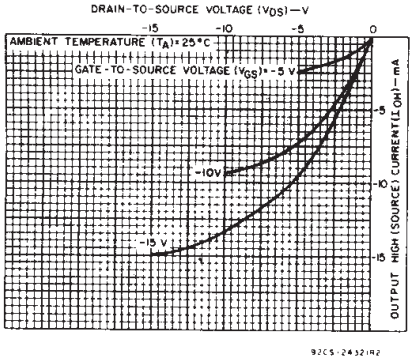


Fig. 10 – Minimum output high (source) current characteristics.

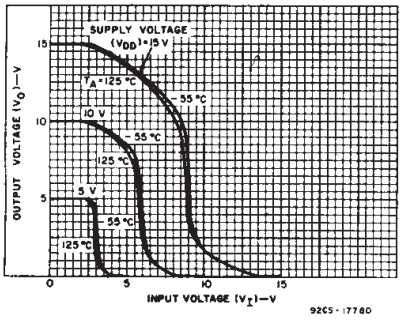


Fig. 11 – Typical voltage-transfer characteristics as a function of temperature.

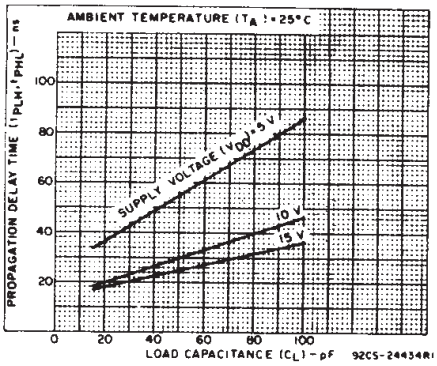


Fig. 12 – Typical propagation delay time vs. load capacitance.

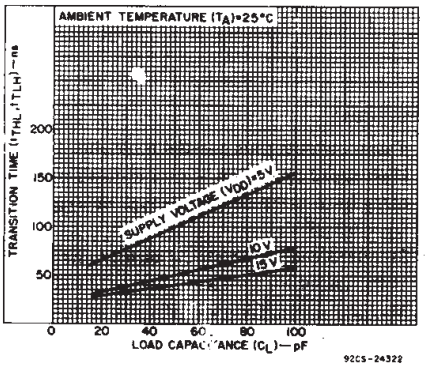


Fig. 13 – Typical transition time vs. load capacitance.

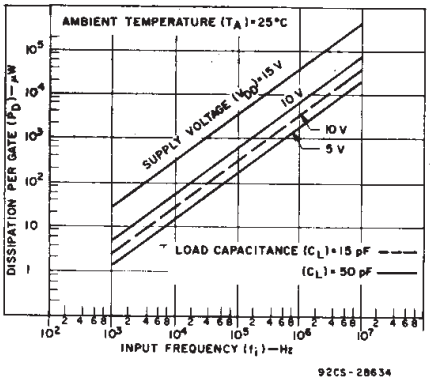


Fig. 14 – Typical dissipation vs. frequency characteristics.

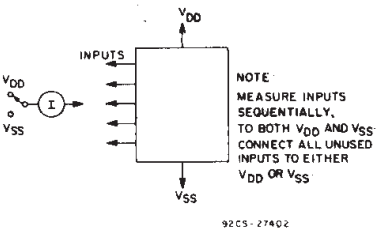


Fig. 15 – Input current test circuit.

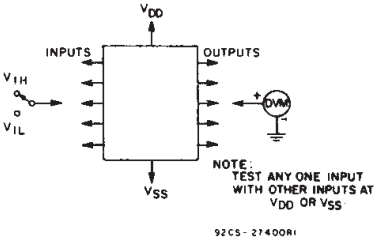


Fig. 16 – Input voltage test circuit.

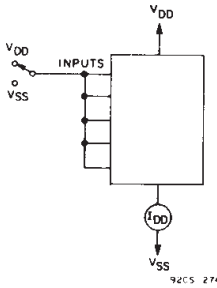
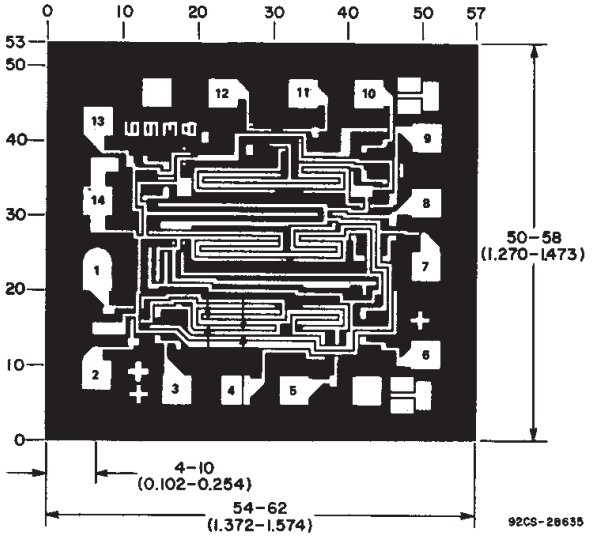


Fig. 17 – Quiescent device current test circuit.



DIMENSIONS AND PAD LAYOUT FOR CD4007UBH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD4007UBE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4007UBF	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD4007UBF3A	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD4007UBF3A116	OBSOLETE	CDIP	J	14		None	Call TI	Call TI
CD4007UBM	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4007UBM96	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4007UBMT	ACTIVE	SOIC	D	14	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4007UBNSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4007UBPW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4007UBPWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

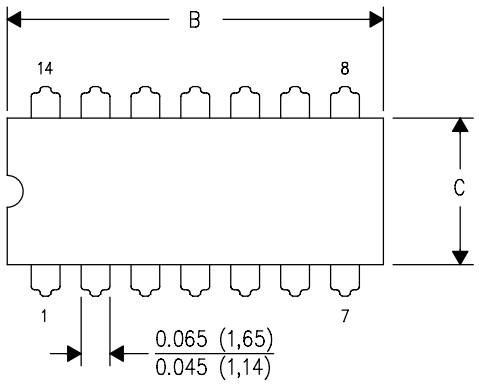
(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

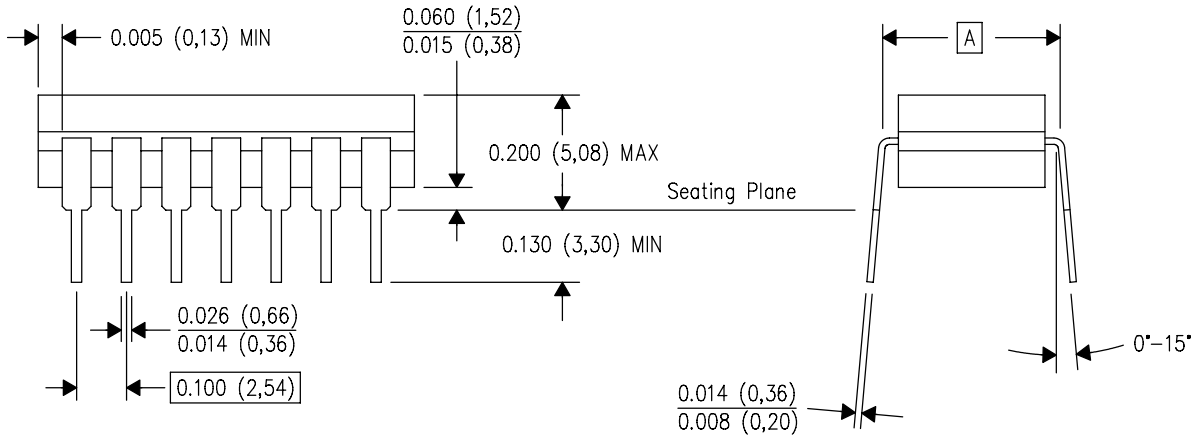
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



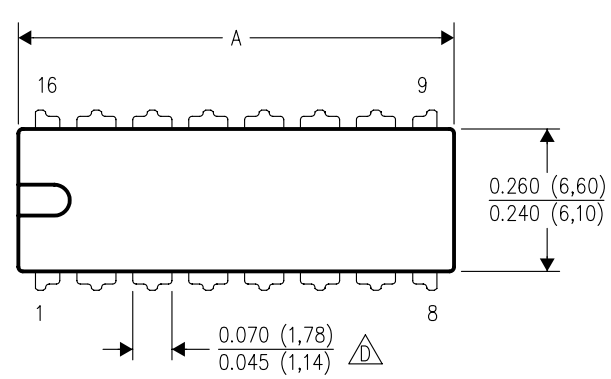
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

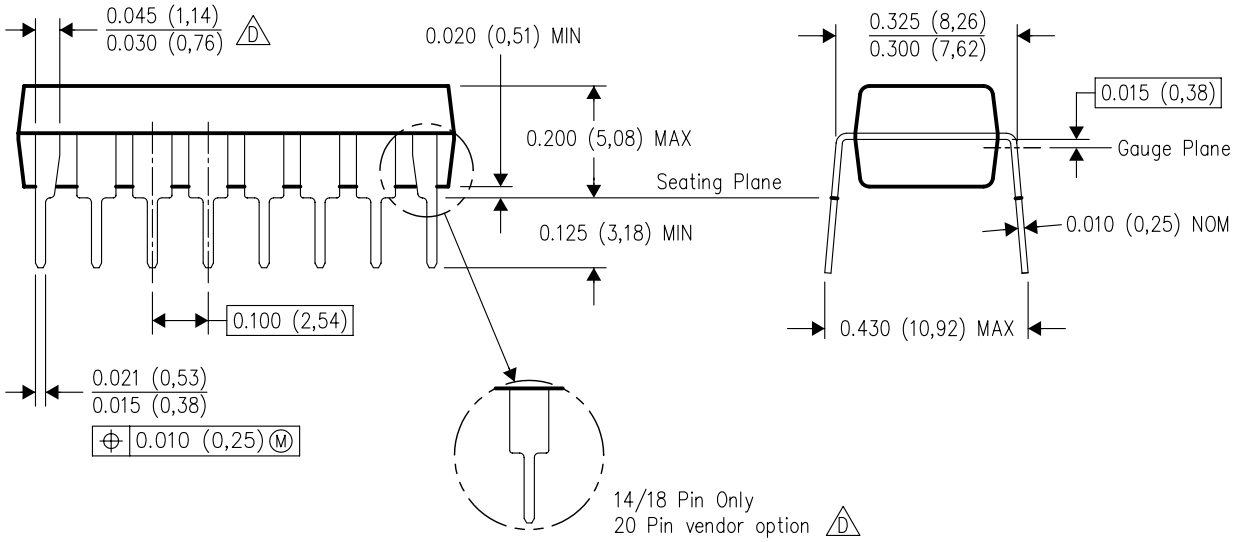
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



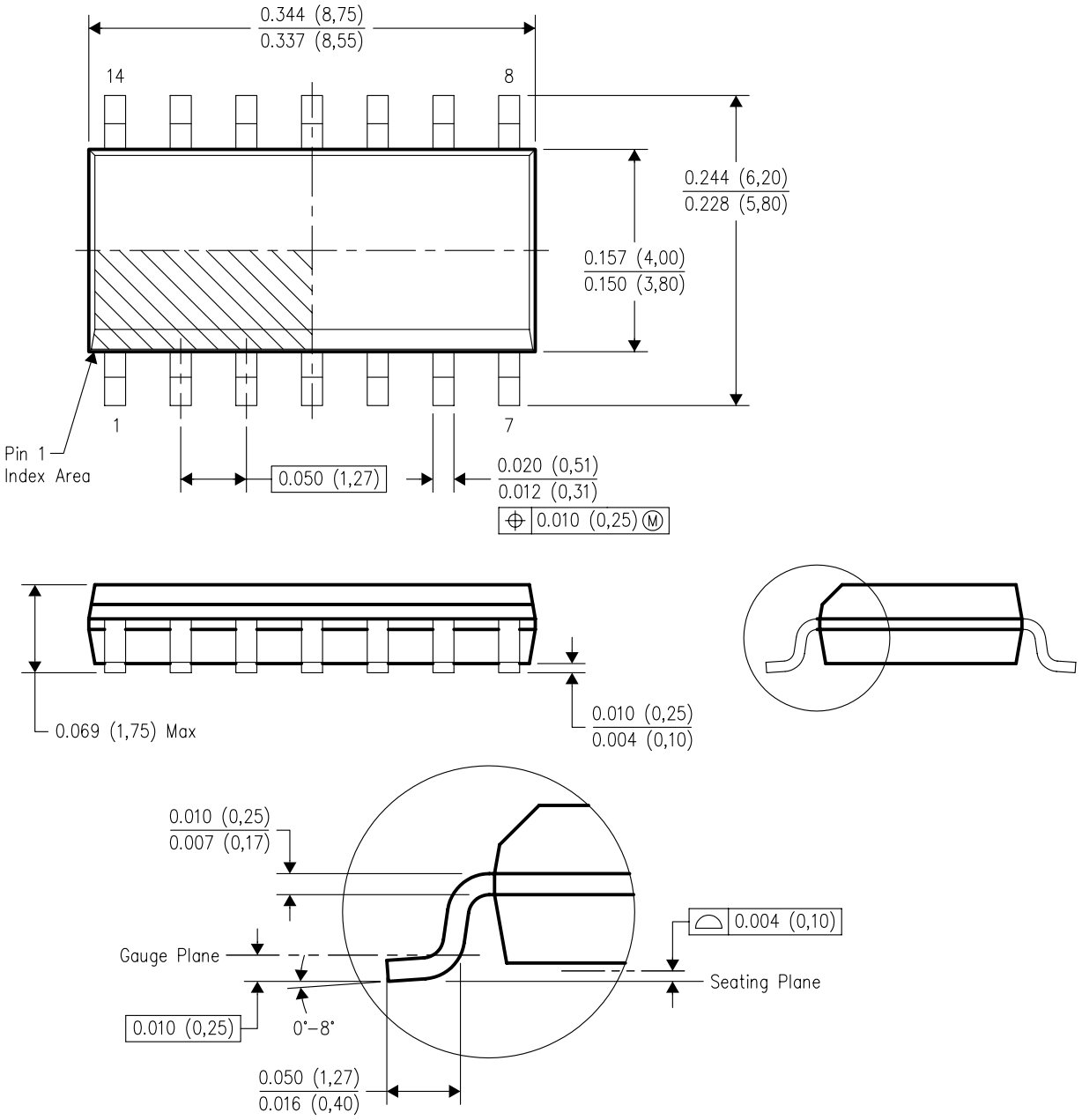
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE

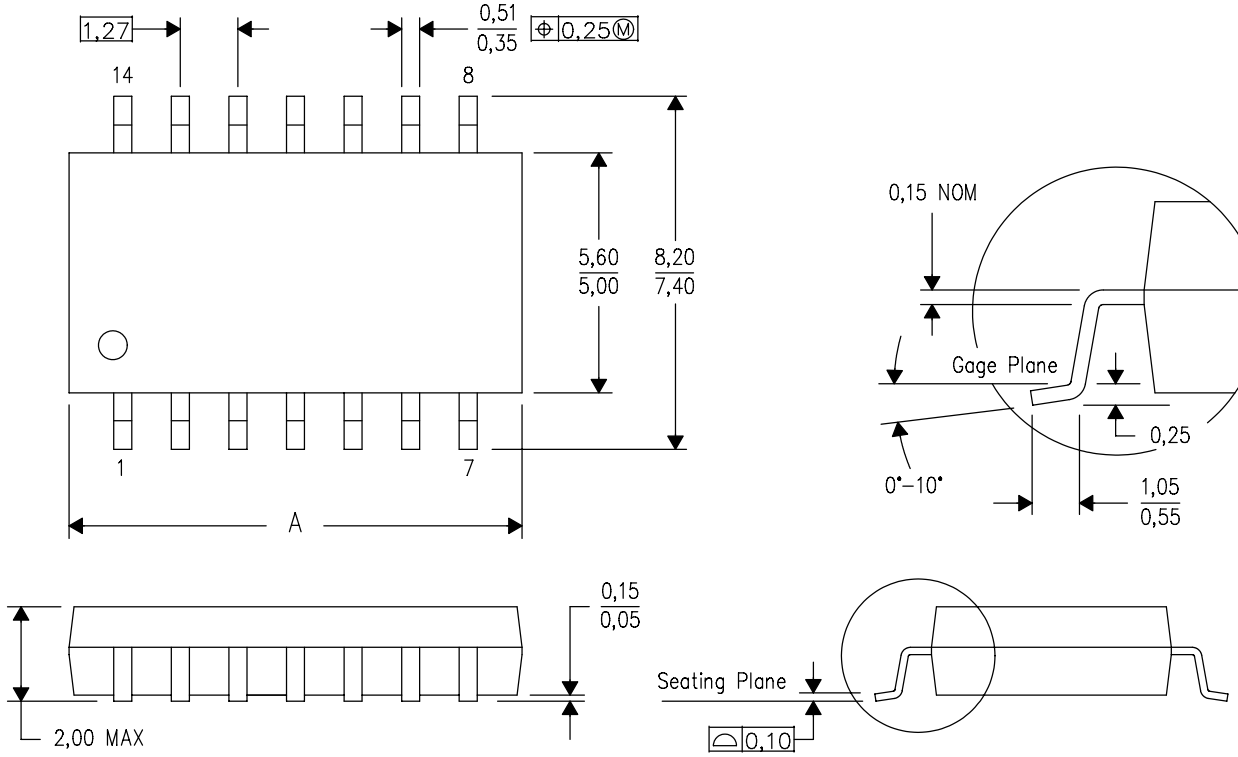


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



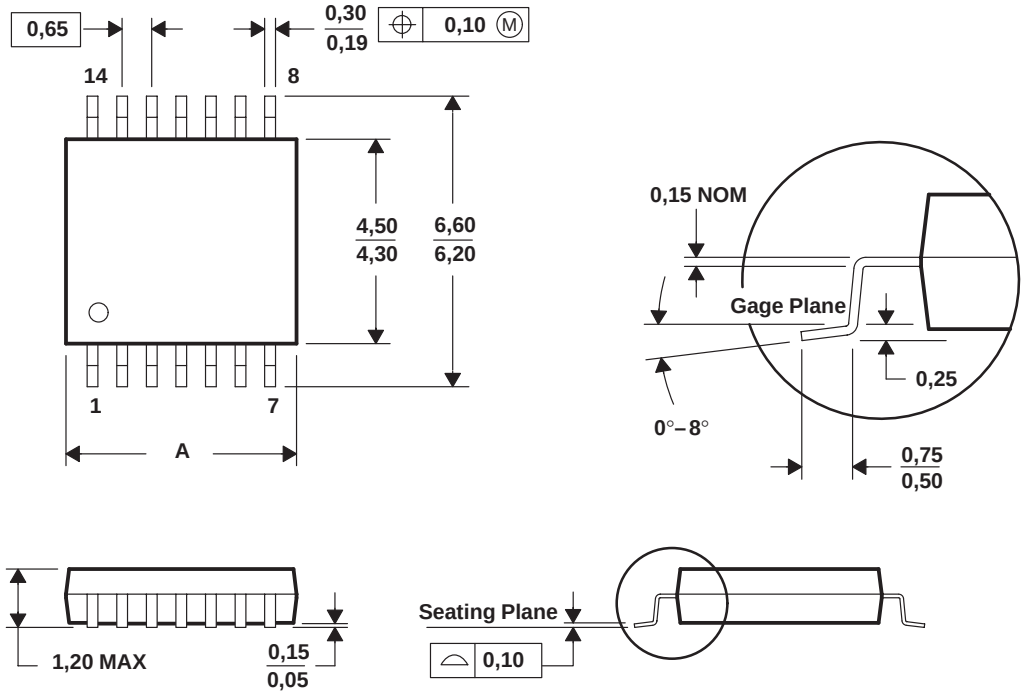
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

CMOS Hex Buffer/Converters

The Harris CD4049UB and CD4050B are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC} = 5V, $V_{OL} \leq 0.4V$, and $I_{OL} \geq 3.3mA$.)

The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because the CD4049UB and CD4050B require only one power supply, they are preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069UB Hex Inverter is recommended.

Features

- CD4049UB Inverting
- CD4050B Non-Inverting
- High Sink Current for Driving 2 TTL Loads
- High-To-Low Level Logic Conversion
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1µA at 18V Over Full Package Temperature Range; 100nA at 18V and 25^{o}C
- 5V, 10V and 15V Parametric Ratings

Applications

- CMOS to DTL/TTL Hex Converter
- CMOS Current “Sink” or “Source” Driver
- CMOS High-To-Low Logic Level Converter

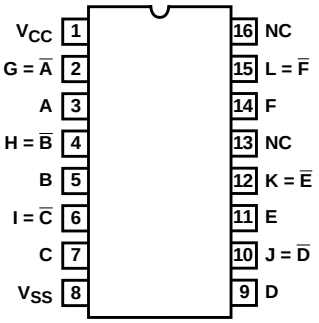
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CD4049UBE	-55 to 125	16 Ld PDIP	E16.3
CD4050BE	-55 to 125	16 Ld PDIP	E16.3
CD4049UBF	-55 to 125	16 Ld CERDIP	F16.3
CD4050BF	-55 to 125	16 Ld CERDIP	F16.3
CD4050BM	-55 to 125	16 Ld SOIC	M16.3

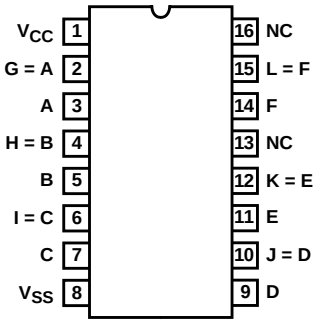
NOTE: Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinouts

CD4049UB (PDIP, CERDIP)
TOP VIEW



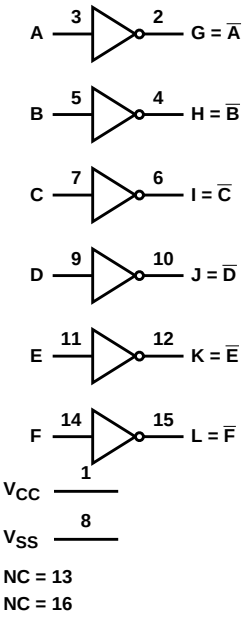
CD4050B (PDIP, CERDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

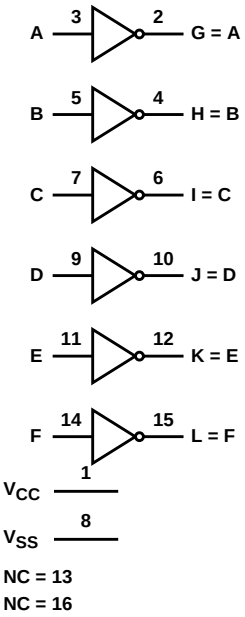
Functional Block Diagrams

CD4049UB



NC = 13
NC = 16

CD4050B



NC = 13
NC = 16

Schematic Diagrams

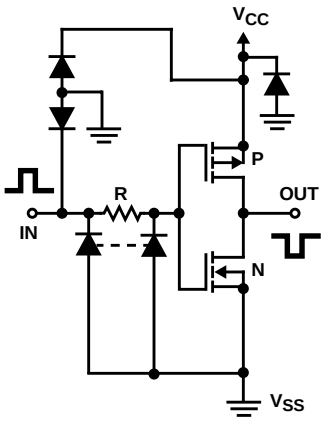


FIGURE 1A. SCHEMATIC DIAGRAM OF CD4049UB, 1 OF 6 IDENTICAL UNITS

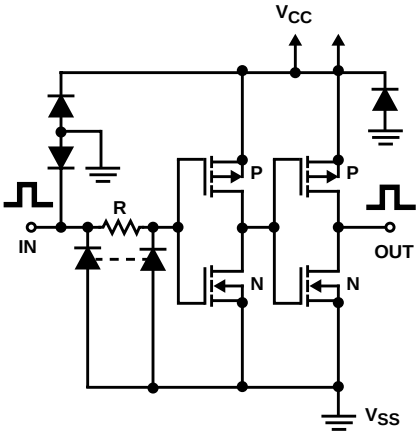


FIGURE 1B. SCHEMATIC DIAGRAM OF CD4050B, 1 OF 6 IDENTICAL UNITS

Absolute Maximum Ratings

Supply Voltage (V+ to V-) . . . . . -0.5V to 20V
DC Input Voltage . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input . . . . . ±10mA

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	90	N/A
CERDIP Package	130	55
SOIC Package	100	N/A

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 265^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURE (^oC)							UNITS
								25			
	V_O (V)	V_{IN} (V)	V_{CC} (V)	-55	-40	85	125	MIN	TYP	MAX	
Quiescent Device Current I_{DD} (Max)	-	0,5	5	1	1	30	30	-	0.02	1	µA
	-	0,10	10	2	2	60	60	-	0.02	2	µA
	-	0,15	15	4	4	120	120	-	0.02	4	µA
	-	0,20	20	20	20	600	600	-	0.04	20	µA
Output Low (Sink) Current I_{OL} (Min)	0.4	0,5	4.5	3.3	3.1	2.1	1.8	2.6	5.2	-	mA
	0.4	0,5	5	4	3.8	2.9	2.4	3.2	6.4	-	mA
	0.5	0,10	10	10	9.6	6.6	5.6	8	16	-	mA
	1.5	0,15	15	26	25	20	18	24	48	-	mA
Output High (Source) Current I_{OH} (Min)	4.6	0,5	5	-0.81	-0.73	-0.58	-0.48	-0.65	-1.2	-	mA
	2.5	0,5	5	-2.6	-2.4	-1.9	-1.55	-2.1	-3.9	-	mA
	9.5	0,10	10	-2.0	-1.8	-1.35	-1.18	-1.65	-3.0	-	mA
	13.5	0,15	15	-5.2	-4.8	-3.5	-3.1	-4.3	-8.0	-	mA
Out Voltage Low Level V_{OL} (Max)	-	0,5	5	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0,10	10	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0,15	5	0.05	0.05	0.05	0.05	-	0	0.05	V
Output Voltage High Level V_{OH} (Min)	-	0,5	5	4.95	4.95	4.95	4.95	4.95	5	-	V
	-	0,10	10	9.95	9.95	9.95	9.95	9.95	10	-	V
	-	0,15	15	14.95	14.95	14.95	14.95	14.95	15	-	V
Input Low Voltage, V_{IL} (Max) CD4049UB	4.5	-	5	1	1	1	1	-	-	1	V
	9	-	10	2	2	2	2	-	-	2	V
	13.5	-	15	2.5	2.5	2.5	2.5	-	-	2.5	V
Input Low Voltage, V_{IL} (Max) CD4050B	0.5	-	5	1.5	1.5	1.5	1.5	-	-	1.5	V
	1	-	10	3	3	3	3	-	-	3	V
	1.5	-	15	4	4	4	4	-	-	4	V
Input High Voltage, V_{IH} Min CD4049UB	0.5	-	5	4	4	4	4	4	-	-	V
	1	-	10	8	8	8	8	8	-	-	V
	1.5	-	15	12.5	12.5	12.5	12.5	12.5	-	-	V

DC Electrical Specifications (Continued)

PARAMETER	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURE (^oC)							UNITS
								25			
	V_O (V)	V_{IN} (V)	V_{CC} (V)	-55	-40	85	125	MIN	TYP	MAX	
Input High Voltage, V_{IH} Min CD4050B	4.5	-	5	3.5	3.5	3.5	3.5	3.5	-	-	V
	9	-	10	7	7	7	7	7	-	-	V
	13.5	-	15	11	11	11	11	11	-	-	V
Input Current, I_{IN} Max	-	0,18	18	±0.1	±0.1	±1	±1	-	$\pm10^{-5}$	±0.1	µA

AC Electrical Specifications $T_A = 25^oC$, Input t_r, t_f = 20ns, C_L = 50pF, R_L = 200kΩ

PARAMETER	TEST CONDITIONS		LIMITS (ALL PACKAGES)		UNITS
	V_{IN}	V_{CC}	TYP	MAX	
Propagation Delay Time Low to High, t_{PLH} CD4049UB	5	5	60	120	ns
	10	10	32	65	ns
	10	5	45	90	ns
	15	15	25	50	ns
	15	5	45	90	ns
Propagation Delay Time Low to High, t_{PLH} CD4050B	5	5	70	140	ns
	10	10	40	80	ns
	10	5	45	90	ns
	15	15	30	60	ns
	15	5	40	80	ns
Propagation Delay Time High to Low, t_{PHL} CD4049UB	5	5	32	65	ns
	10	10	20	40	ns
	10	5	15	30	ns
	15	15	15	30	ns
	15	5	10	20	ns
Propagation Delay Time High to Low, t_{PHL} CD4050B	5	5	55	110	ns
	10	10	22	55	ns
	10	5	50	100	ns
	15	15	15	30	ns
	15	5	50	100	ns
Transition Time, Low to High, t_{TLH}	5	5	80	160	ns
	10	10	40	80	ns
	15	15	30	60	ns
Transition Time, High to Low, t_{THL}	5	5	30	60	ns
	10	10	20	40	ns
	15	15	15	30	ns
Input Capacitance, C_{IN} CD4049UB	-	-	15	22.5	pF
Input Capacitance, C_{IN} CD4050B	-	-	5	7.5	pF

Typical Performance Curves

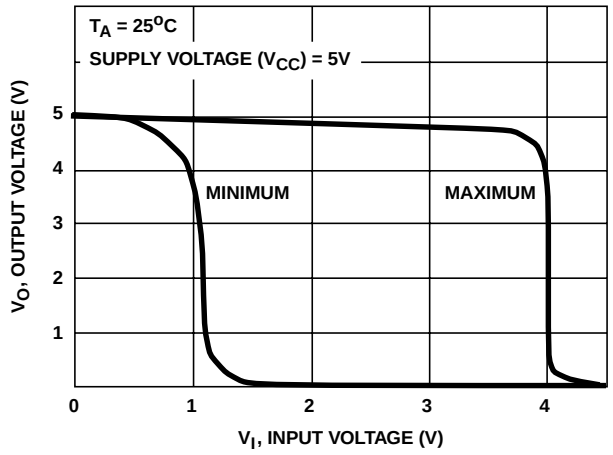


FIGURE 2. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS FOR CD4049UB

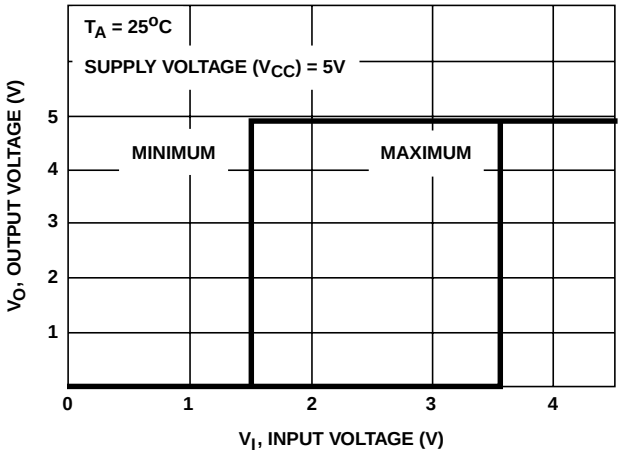


FIGURE 3. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS FOR CD4050B

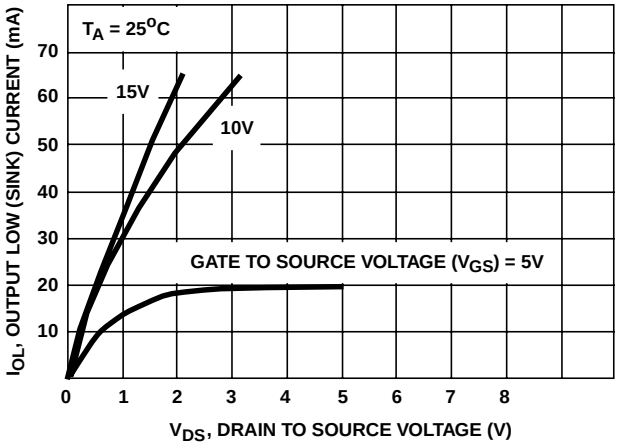


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

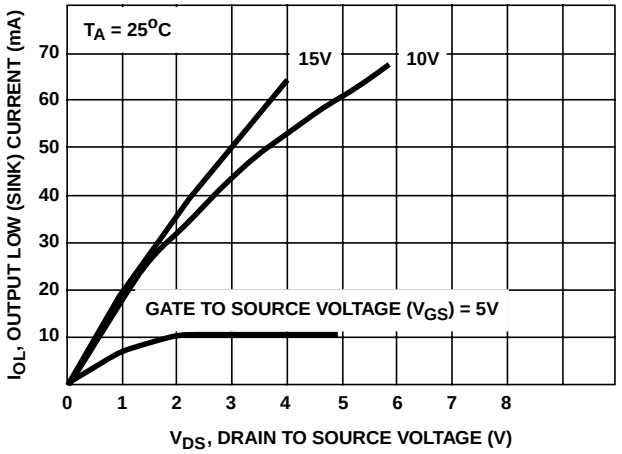


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT DRAIN CHARACTERISTICS

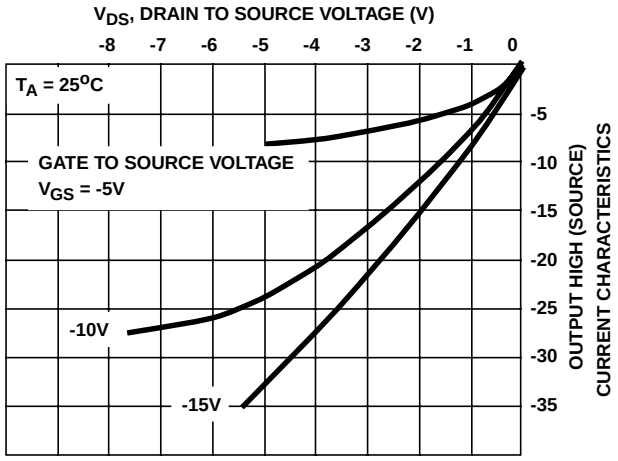


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

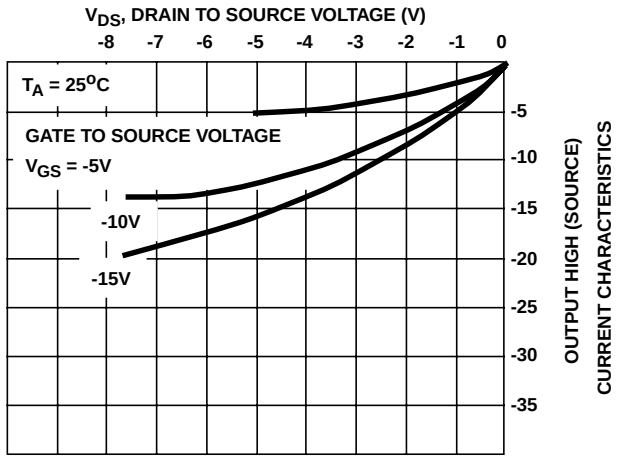


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Curves (Continued)

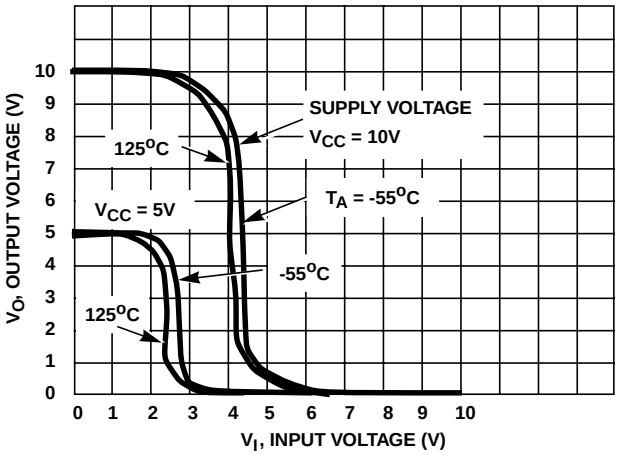


FIGURE 8. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE FOR CD4049UB

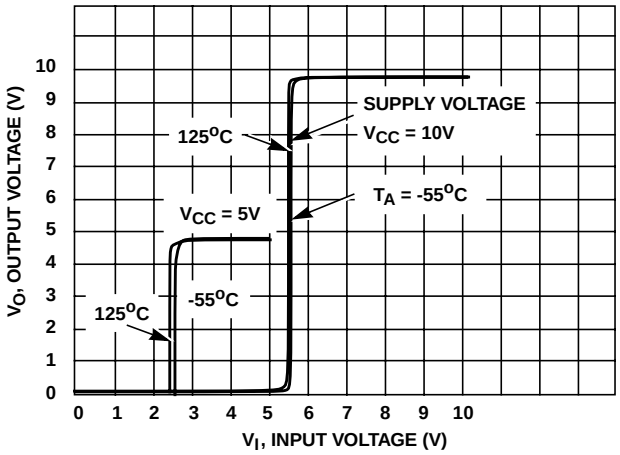


FIGURE 9. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE FOR CD4050B

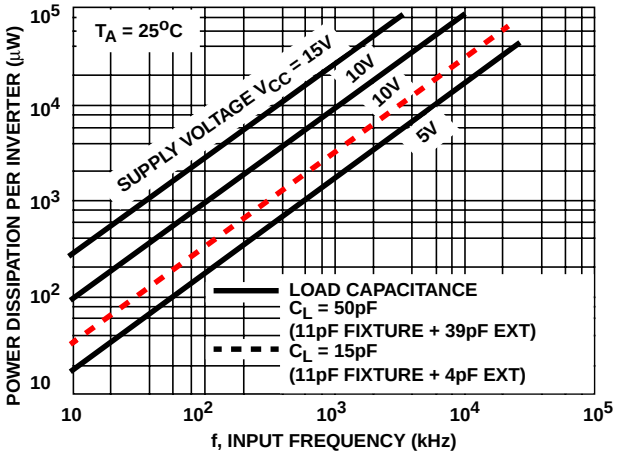


FIGURE 10. TYPICAL POWER DISSIPATION vs FREQUENCY CHARACTERISTICS

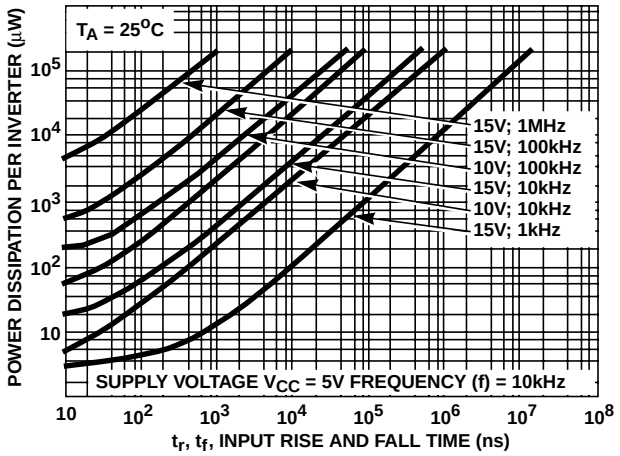


FIGURE 11. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTER FOR CD4049UB

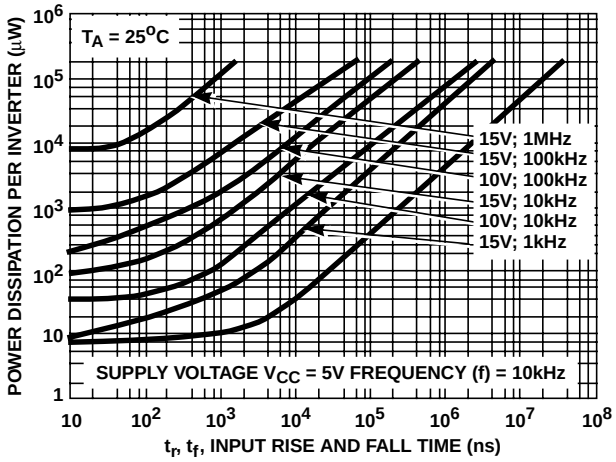


FIGURE 12. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTERFOR CD4050B

Test Circuits

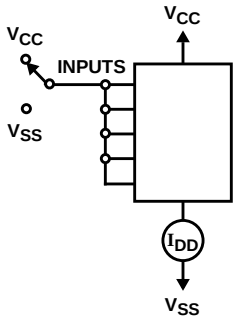
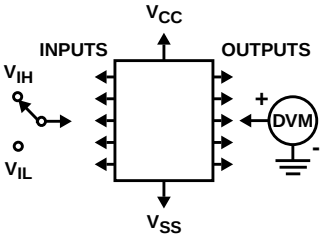
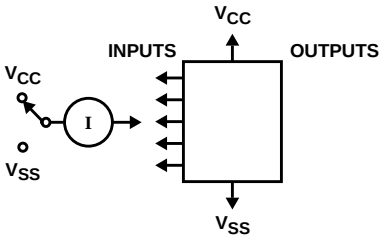


FIGURE 13. QUIESCENT DEVICE CURRENT TEST CIRCUIT



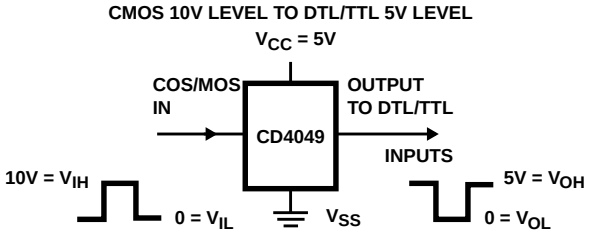
NOTE: Test any one input with other inputs at V_{CC} or V_{SS}.

FIGURE 14. INPUT VOLTAGE TEST CIRCUIT



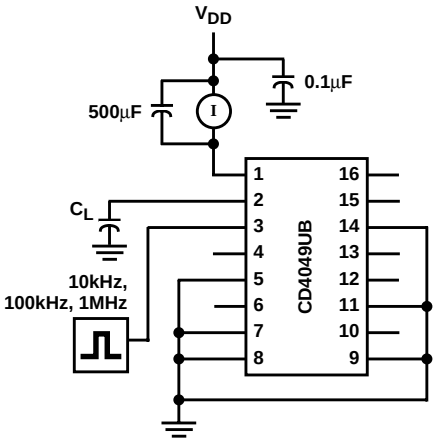
NOTE: Measure inputs sequentially, to both V_{CC} and V_{SS} connect all unused inputs to either V_{CC} or V_{SS}.

FIGURE 15. INPUT CURRENT TEST CIRCUIT



In Terminal - 3, 5, 7, 9, 11, or 14
Out Terminal - 2, 4, 6, 10, 12 or 15
V_{CC} Terminal - 1
V_{SS} Terminal - 8

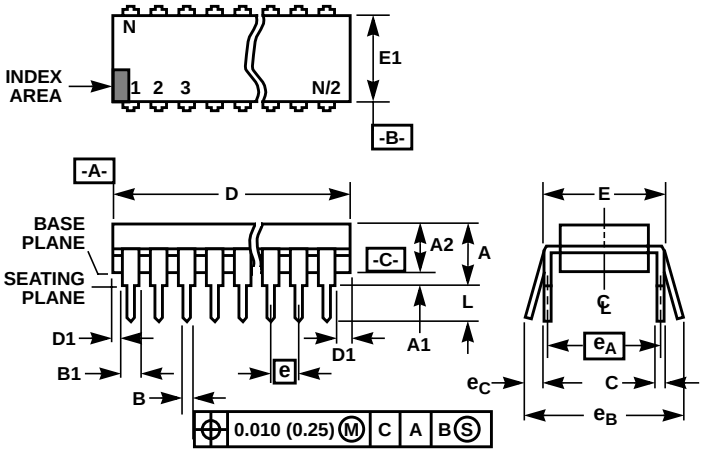
FIGURE 16. LOGIC LEVEL CONVERSION APPLICATION



C_L INCLUDES FIXTURE CAPACITANCE

FIGURE 17. DYNAMIC POWER DISSIPATION TEST CIRCUITS

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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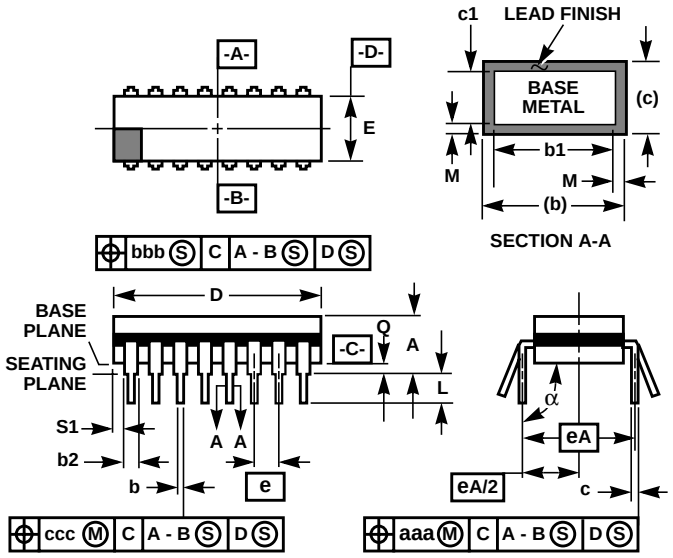
Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

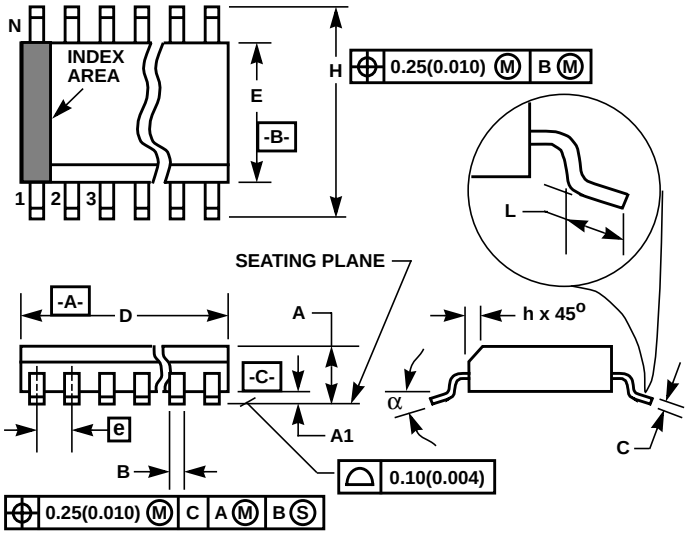
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

Rev. 0 4/94

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

FAIRCHILD SEMICONDUCTOR™

November 1988
Revised November 1999

74AC00 • 74ACT00
Quad 2-Input NAND Gate

General Description

The AC/ACT00 contains four 2-input NAND gates.

Features

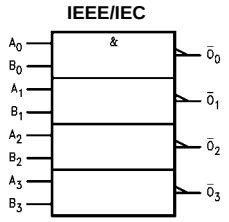
- I_{CC} reduced by 50%
- Outputs source/sink 24 mA
- ACT00 has TTL-compatible inputs

Ordering Code:

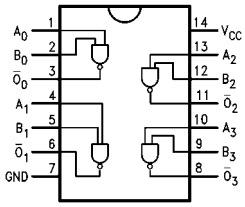
Order Number	Package Number	Package Description
74AC00SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74AC00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ Type II, 5.3mm Wide
74AC00MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC00PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT00SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74ACT00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ Type II, 5.3mm Wide
74ACT00MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT00PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering form. (PC not available in Tape and Reel.)

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC}	T_A = +25°C	T_A = −40°C to +85°C		Units	Conditions
		(V)	Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level	3.0	1.5	2.1	2.1		V_{OUT} = 0.1V
	Input Voltage	4.5	2.25	3.15	3.15	V	or V_{CC} − 0.1V
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level	3.0	1.5	0.9	0.9		V_{OUT} = 0.1V
	Input Voltage	4.5	2.25	1.35	1.35	V	or V_{CC} − 0.1V
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level	3.0	2.99	2.9	2.9		
	Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.46		I_{OH} = −12 mA
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 2)
V_{OL}	Maximum LOW Level	3.0	0.002	0.1	0.1		
	Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.44		I_{OL} = 12 mA
		4.5		0.36	0.44	V	I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 2)
I_{IN} (Note 3)	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	Minimum Dynamic	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 4)	5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC} (Note 3)	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	V_{IN} = V_{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC}	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$		Units	Conditions
		(V)	Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24$ mA
		5.5		4.86	4.76		$I_{OH} = -24$ mA (Note 5)
V_{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24$ mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 5)
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Minimum Dynamic Output Current (Note 6)	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V) (Note 7)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	3.3	2.0	7.0	9.5	2.0	10.0	ns
		5.0	1.5	6.0	8.0	1.5	8.5	
t_{PHL}	Propagation Delay	3.3	1.5	5.5	8.0	1.0	8.5	ns
		5.0	1.5	4.5	6.5	1.0	7.0	

Note 7: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

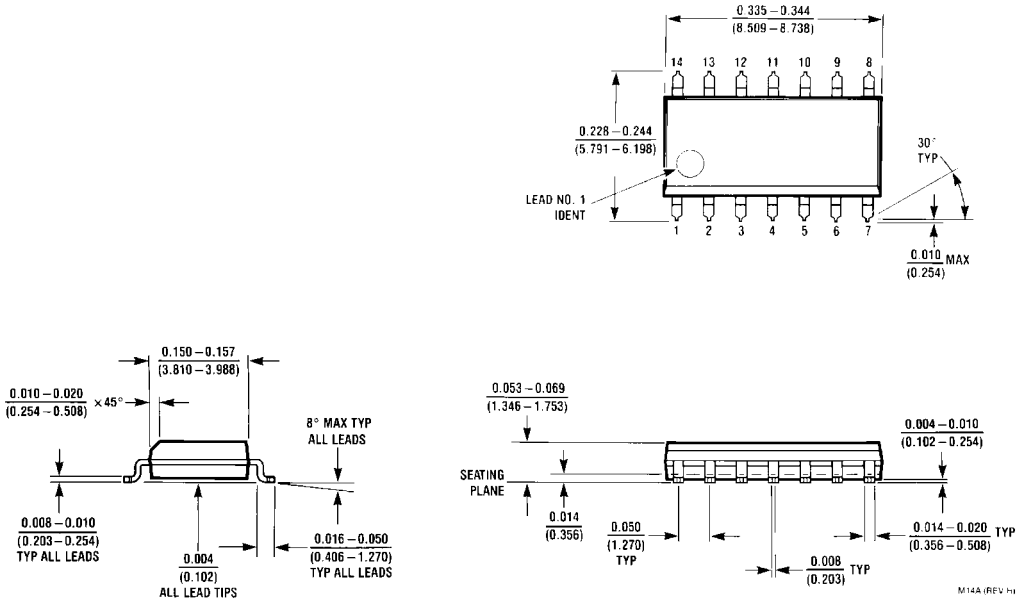
Symbol	Parameter	V_{CC} (V) (Note 8)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	5.0	1.5	5.5	9.0	1.0	9.5	ns
t_{PHL}	Propagation Delay	5.0	1.5	4.0	7.0	1.0	8.0	ns

Note 8: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

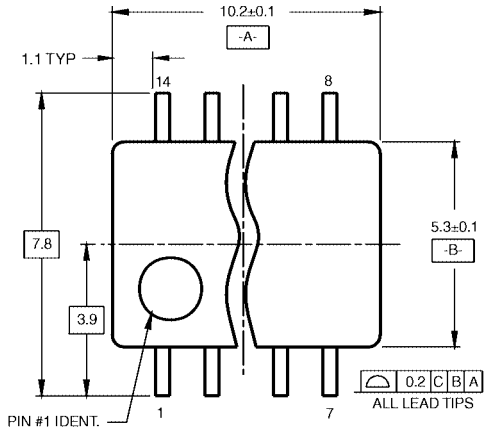
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance	30.0	pF	$V_{CC} = 5.0V$

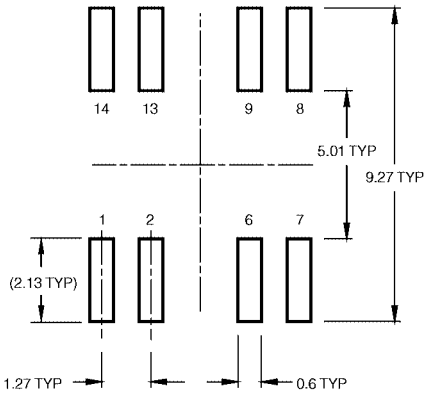
Physical Dimensions inches (millimeters) unless otherwise noted



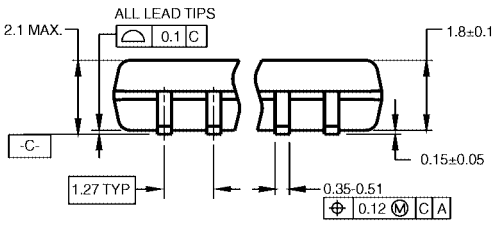
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150” Narrow Body
Package Number M14A

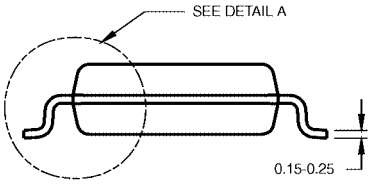
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



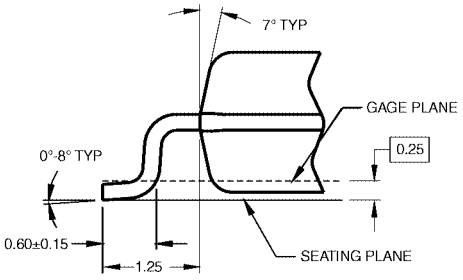


LAND PATTERN RECOMMENDATION





DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

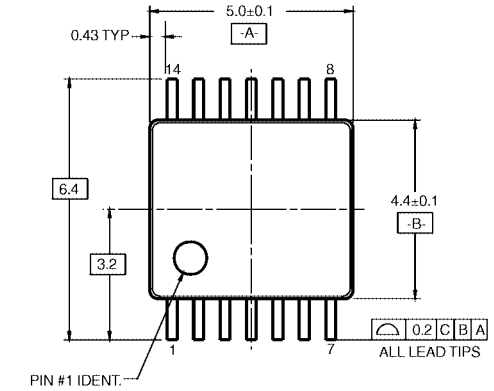
B. DIMENSIONS ARE IN MILLIMETERS.

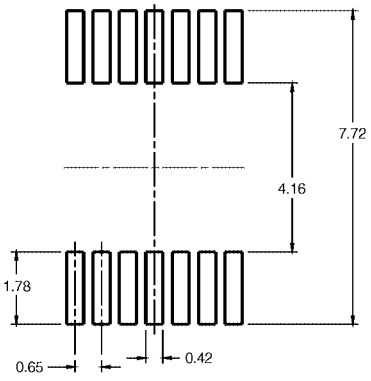
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

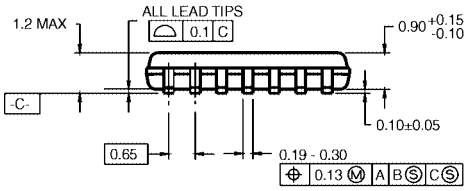
14-Lead Small Outline Package (SOIC), EIAJ Type II, 5.3mm Wide
Package Number M14D

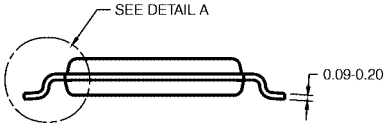
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

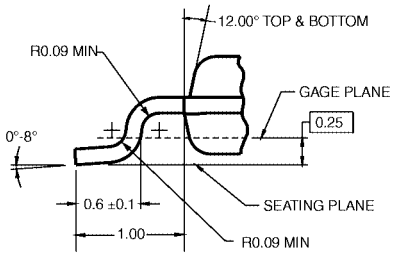




LAND PATTERN RECOMMENDATION







DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

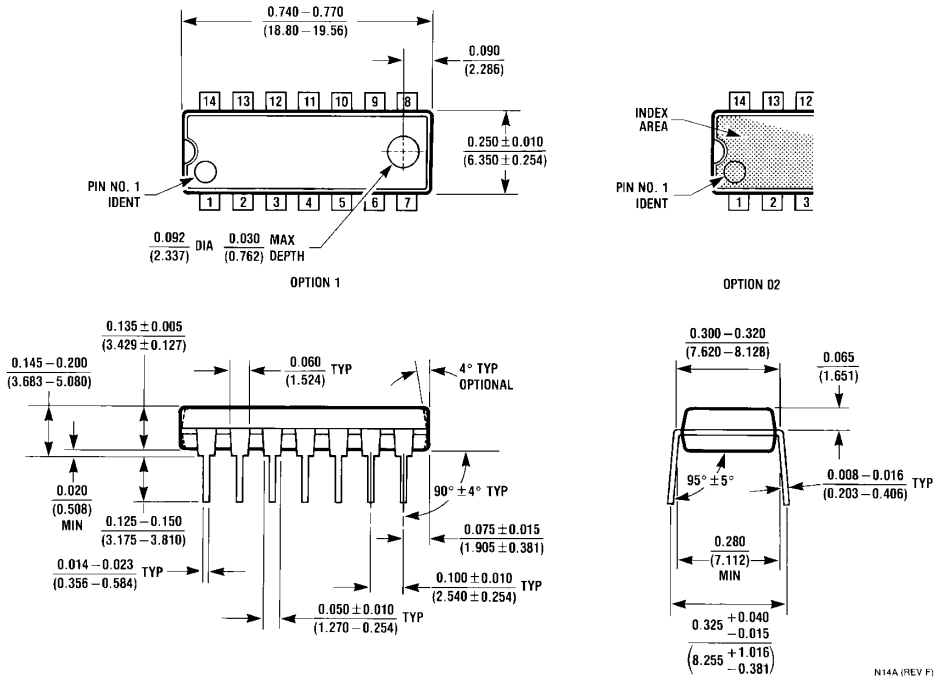
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153,4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

DATA SHEET

74HC04; 74HCT04
Hex inverter

Product specification
Supersedes data of 1993 Sep 01

2003 Jul 23

Philips
Semiconductors

PHILIPS

FEATURES

- Complies with JEDEC standard no. 8-1A
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74HC/HCT04 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT04 provide six inverting buffers.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 6.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC04	HCT04	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	7	8	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	21	24	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. For 74HC04: the condition is V_I = GND to V_{CC}.
   For 74HCT04: the condition is V_I = GND to V_{CC} – 1.5 V.

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
nA	nY
L	H
H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC04N	–40 to +125 °C	14	DIP14	plastic	SOT27-1
74HCT04N	–40 to +125 °C	14	DIP14	plastic	SOT27-1
74HC04D	–40 to +125 °C	14	SO14	plastic	SOT108-1
74HCT04D	–40 to +125 °C	14	SO14	plastic	SOT108-1
74HC04DB	–40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HCT04DB	–40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HC04PW	–40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HCT04PW	–40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HC04BQ	–40 to +125 °C	14	DHVQFN14	plastic	SOT762-1
74HCT04BQ	–40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1Y	data output
3	2A	data input
4	2Y	data output
5	3A	data input
6	3Y	data output
7	GND	ground (0 V)
8	4Y	data output
9	4A	data input
10	5Y	data output
11	5A	data input
12	6Y	data output
13	6A	data input
14	V_{CC}	supply voltage

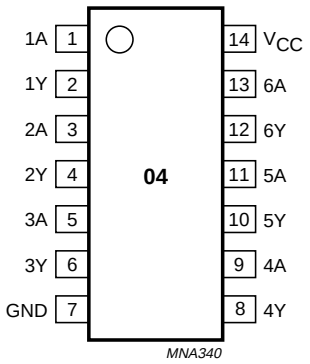
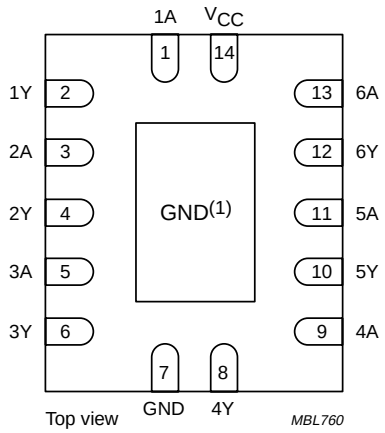


Fig.1 Pin configuration DIP14, SO14 and (T)SSOP14.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

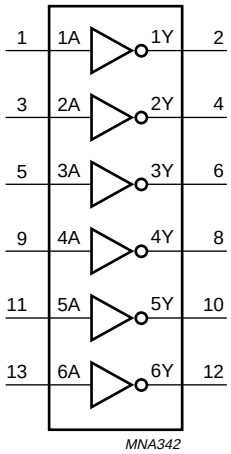


Fig.3 Logic symbol.

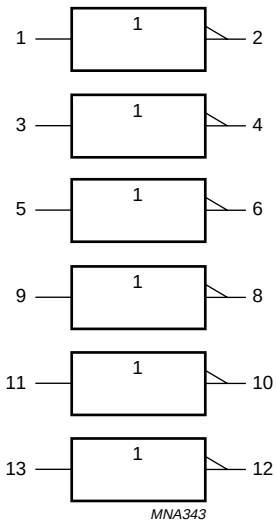


Fig.4 IEC logic symbol.

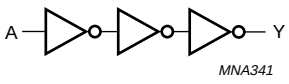


Fig.5 Logic diagram (one inverter).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC04			74HCT04			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	–	–	1000	–	–	–	ns
		V_{CC} = 4.5 V	–	6.0	500	–	6.0	500	ns
		V_{CC} = 6.0 V	–	–	400	–	–	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	–	±20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	–	±20	mA
I_O	output source or sink current	-0.5 V $< V_O < V_{CC} + 0.5$ V	–	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation				
	DIP14 package	T_{amb} = –40 to +125 °C; note 1	–	750	mW
	other packages	T_{amb} = –40 to +125 °C; note 2	–	500	mW

Notes

1. For DIP14 packages: above 70 °C derate linearly with 12 mW/K.
2. For SO14 packages: above 70 °C derate linearly with 8 mW/K.
   For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
   For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

DC CHARACTERISTICS

Type 74HC04

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = 25 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V_{IL}	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –20 μA	2.0	1.9	2.0	–	V
		I_O = –20 μA	4.5	4.4	4.5	–	V
		I_O = –4.0 mA	4.5	3.98	4.32	–	V
		I_O = –20 μA	6.0	5.9	6.0	–	V
		I_O = –5.2 mA	6.0	5.48	5.81	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 μA	2.0	–	0	0.1	V
		I_O = 20 μA	4.5	–	0	0.1	V
		I_O = 4.0 mA	4.5	–	0.15	0.26	V
		I_O = 20 μA	6.0	–	0	0.1	V
		I_O = 5.2 mA	6.0	–	0.16	0.26	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	6.0	–	0.1	±0.1	μA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	6.0	–	–	±.0.5	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	6.0	–	–	2	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –20 μA	2.0	1.9	–	–	V
		I_O = –20 μA	4.5	4.4	–	–	V
		I_O = –4.0 mA	4.5	3.84	–	–	V
		I_O = –20 μA	6.0	5.9	–	–	V
		I_O = –5.2 mA	6.0	5.34	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 μA	2.0	–	–	0.1	V
		I_O = 20 μA	4.5	–	–	0.1	V
		I_O = 4.0 mA	4.5	–	–	0.33	V
		I_O = 20 μA	6.0	–	–	0.1	V
		I_O = 5.2 mA	6.0	–	–	0.33	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	6.0	–	–	±1.0	μA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	6.0	–	–	±.5.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	6.0	–	–	20	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –20 μA	2.0	1.9	–	–	V
		I_O = –20 μA	4.5	4.4	–	–	V
		I_O = –20 μA	6.0	5.9	–	–	V
		I_O = –4.0 mA	4.5	3.7	–	–	V
		I_O = –5.2 mA	6.0	5.2	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 μA	2.0	–	–	0.1	V
		I_O = 20 μA	4.5	–	–	0.1	V
		I_O = 20 μA	6.0	–	–	0.1	V
		I_O = 4.0 mA	4.5	–	–	0.4	V
		I_O = 5.2 mA	6.0	–	–	0.4	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	6.0	–	–	±1.0	μA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	6.0	–	–	±10.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	6.0	–	–	40	μA

Type 74HCT04

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = 25 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –20 μA	4.5	4.4	4.5	–	V
		I_O = –4.0 mA	4.5	3.84	4.32	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 μA	4.5	–	0	0.1	V
		I_O = 4.0 mA	4.5	–	0.15	0.26	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	±0.1	μA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; I_O = 0	5.5	–	–	±0.5	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	2	μA
ΔI_{CC}	additional supply current per input	V_I = V_{CC} – 2.1 V; I_O = 0	4.5 to 5.5	–	120	432	μA
T_{amb} = –40 to +85 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}			–		
		I_O = –20 μA	4.5	4.4	–	–	V
		I_O = –4.0 mA	4.5	3.84	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}			–		
		I_O = 20 μA	4.5	–	–	0.1	V
		I_O = 4.0 mA	4.5	–	–	0.33	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	±1.0	μA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; I_O = 0	5.5	–	–	±5.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	20	μA
ΔI_{CC}	additional supply current per input	V_I = V_{CC} – 2.1 V; I_O = 0	4.5 to 5.5	–	–	540	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –20 μA	4.5	4.4	–	–	V
		I_O = –4.0 mA	4.5	3.7	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 μA	4.5	–	–	0.1	V
		I_O = 4.0 mA	4.5	–	–	0.4	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	±1.0	μA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; I_O = 0	5.5	–	–	±10	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	40	μA
ΔI_{CC}	additional supply current per input	V_I = V_{CC} – 2.1 V; I_O = 0	4.5 to 5.5	–	–	590	μA

AC CHARACTERISTICS

Family 74HC04

GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

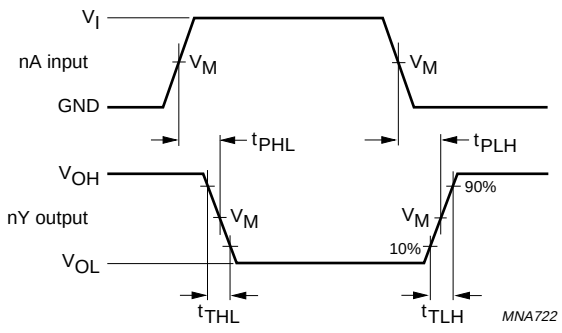
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = 25 °C							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	2.0	–	25	85	ns
			4.5	–	9	17	ns
			6.0	–	7	14	ns
t_{THL}/t_{TLH}	output transition time	see Figs 6 and 7	2.0	–	19	75	ns
			4.5	–	7	15	ns
			6.0	–	6	13	ns
T_{amb} = −40 to +85 °C							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	2.0	–	–	105	ns
			4.5	–	–	21	ns
			6.0	–	–	18	ns
t_{THL}/t_{TLH}	output transition time	see Figs 6 and 7	2.0	–	–	95	ns
			4.5	–	–	19	ns
			6.0	–	–	16	ns
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	2.0	–	–	130	ns
			4.5	–	–	26	ns
			6.0	–	–	22	ns
t_{THL}/t_{TLH}	output transition time	see Figs 6 and 7	2.0	–	–	110	ns
			4.5	–	–	22	ns
			6.0	–	–	19	ns

Family 74HCT04

GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

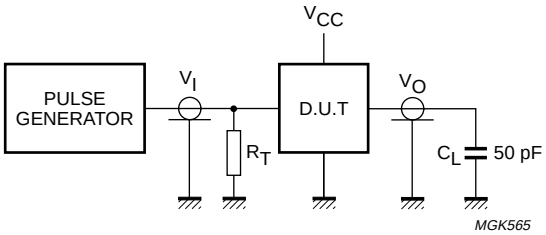
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = 25 °C							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	4.5	–	10	19	ns
t_{THL}/t_{TLH}	output transition time	see Figs 6 and 7	4.5	–	7	15	ns
T_{amb} = −40 to +85 °C							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	4.5	–	–	24	ns
t_{THL}/t_{TLH}	output transition time	see Figs 6 and 7	4.5	–	–	19	ns
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	4.5	–	–	29	ns
t_{THL}/t_{TLH}	output transition time	see Figs 6 and 7	4.5	–	–	22	ns

AC WAVEFORMS



For 74HC04: V_M = 50%; V_I = GND to V_{CC}.
For 74HCT04: V_M = 1.3 V; V_I = GND to 3.0 V.

Fig.6 Waveforms showing the data input (nA) to data output (nY) propagation delays and the output transition times.



Definitions for test circuit:

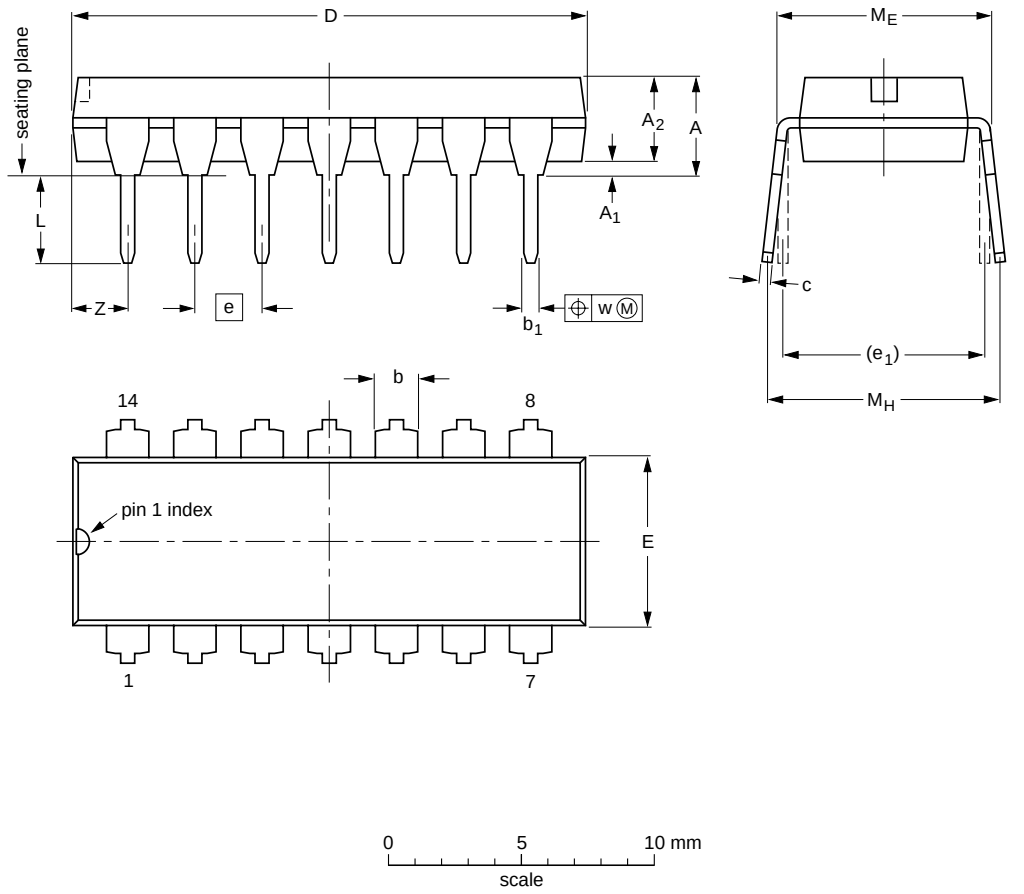
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

PACKAGE OUTLINES

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

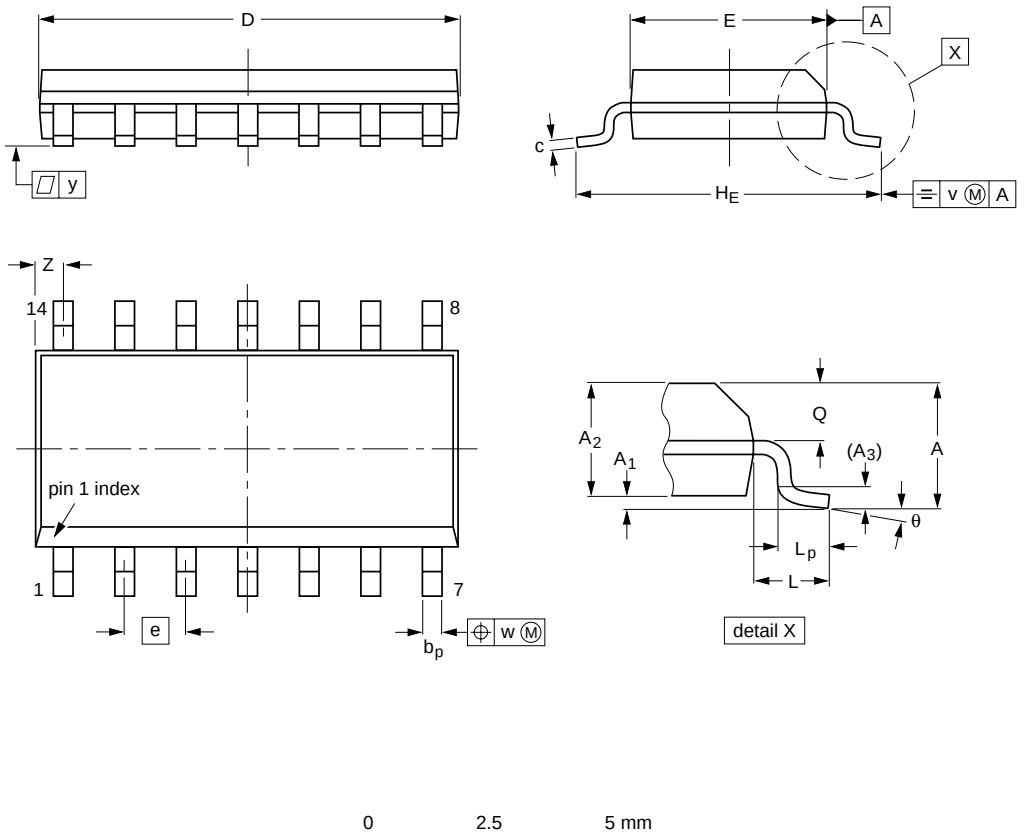
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

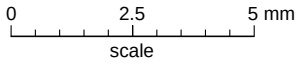
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

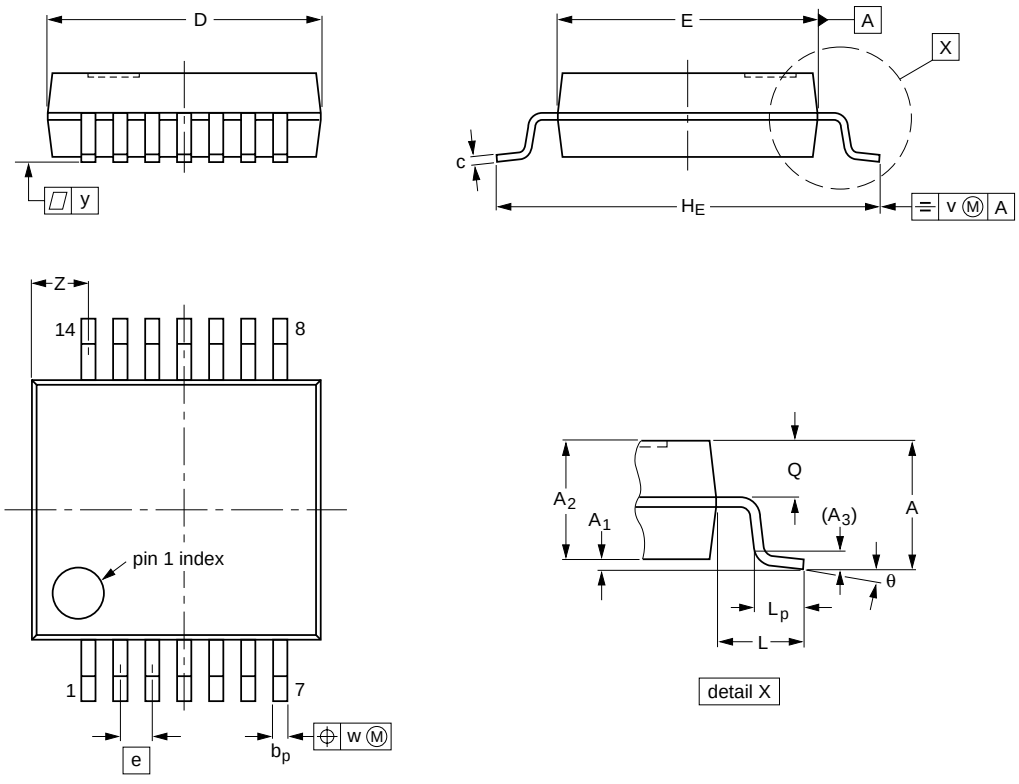
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

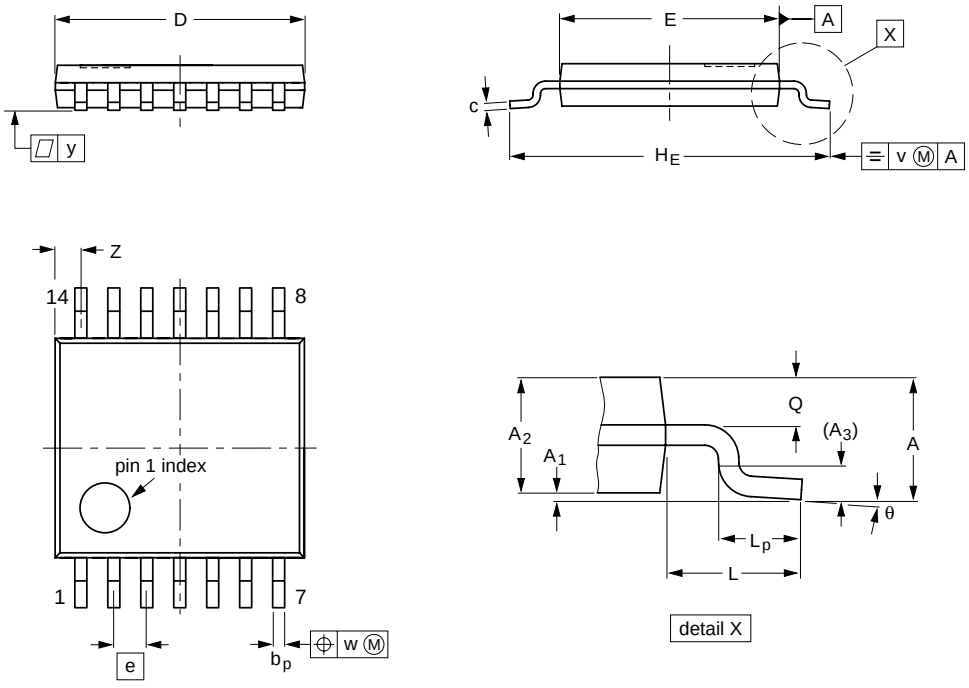
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

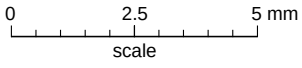
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**





DIMENSIONS (mm are the original dimensions)

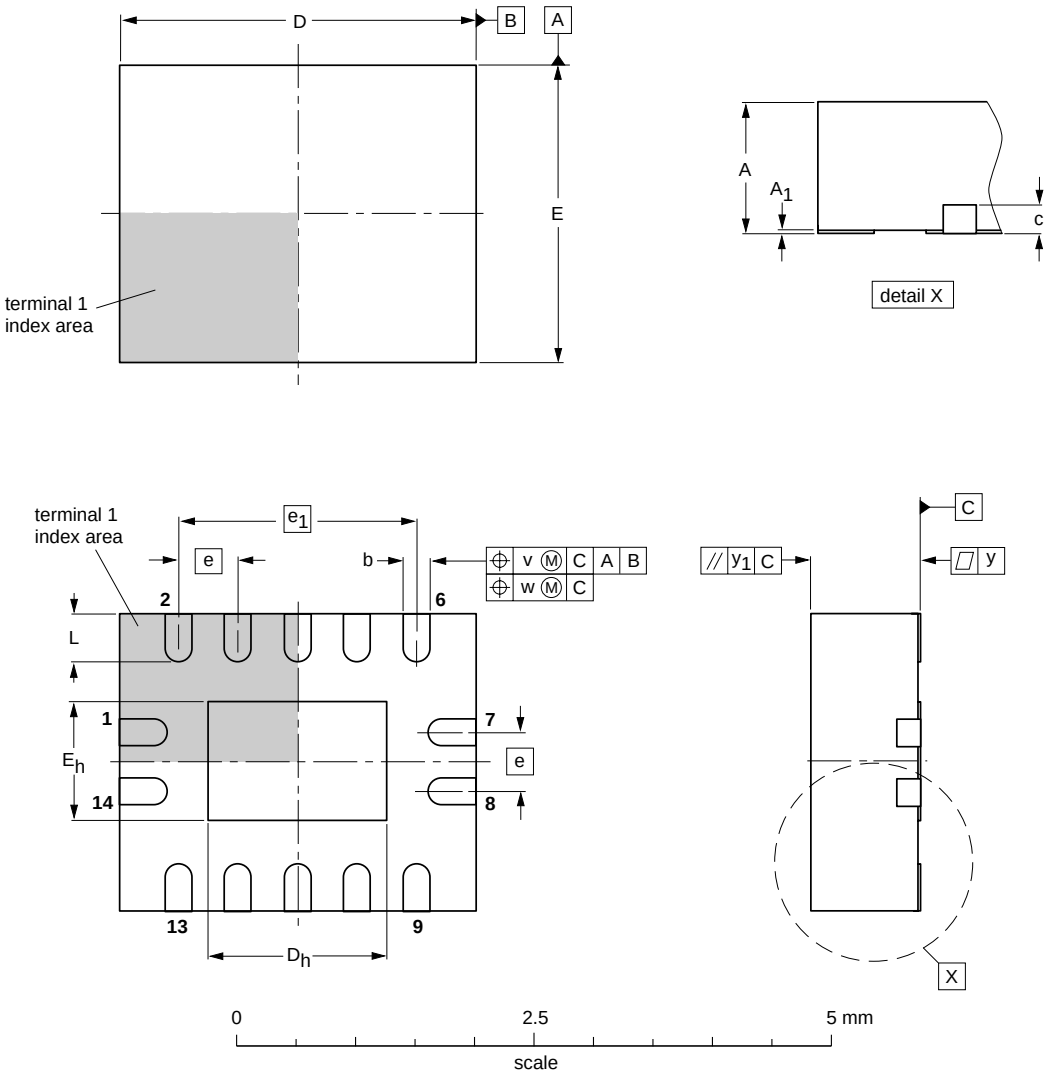
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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MOTOROLA

SN54/74LS112A

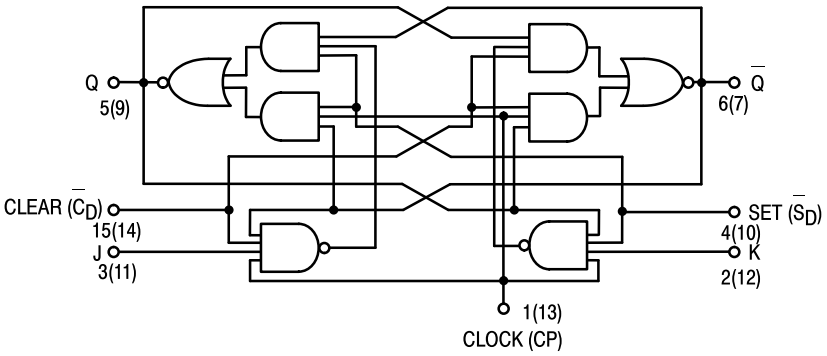
DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

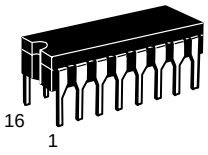
The SN54/74LS112A dual JK flip-flop features individual J, K, clock, and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

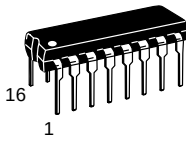
LOW POWER SCHOTTKY

LOGIC DIAGRAM (Each Flip-Flop)

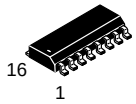




J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

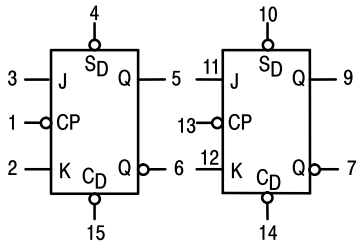
MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S_D}$	$\overline{C_D}$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	q	q
Load “0” (Reset)	H	H	l	h	L	H
Load “1” (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	q

* Both outputs will be HIGH while both S_D and C_D are LOW, but the output states are unpredictable if S_D and C_D go HIGH simultaneously.

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don’t Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current	J, K Set, Clear Clock			20 60 80	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		J, K Set, Clear Clock			0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	J, K Clear, Set, Clk			−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				6.0	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

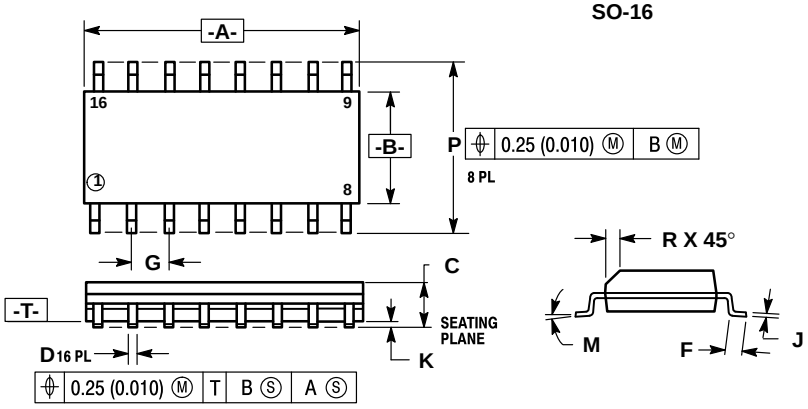
AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	30	45		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock Clear, Set to Output		15	20	ns	
			15	20	ns	

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_W	Clock Pulse Width High	20			ns	V_{CC} = 5.0 V
t_W	Clear, Set Pulse Width	25			ns	
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

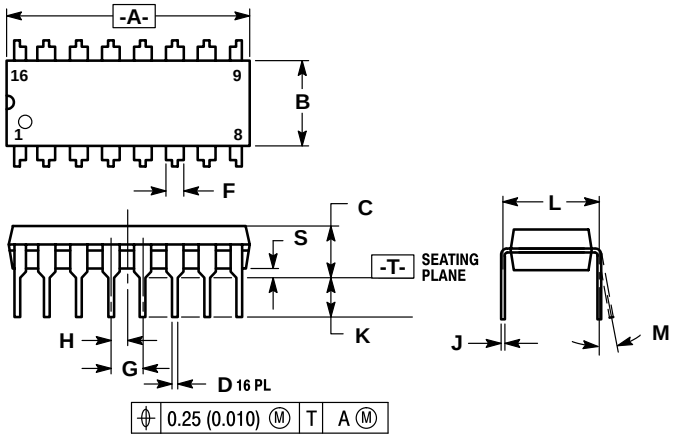
Case 751B-03 D Suffix
16-Pin Plastic
SO-16



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

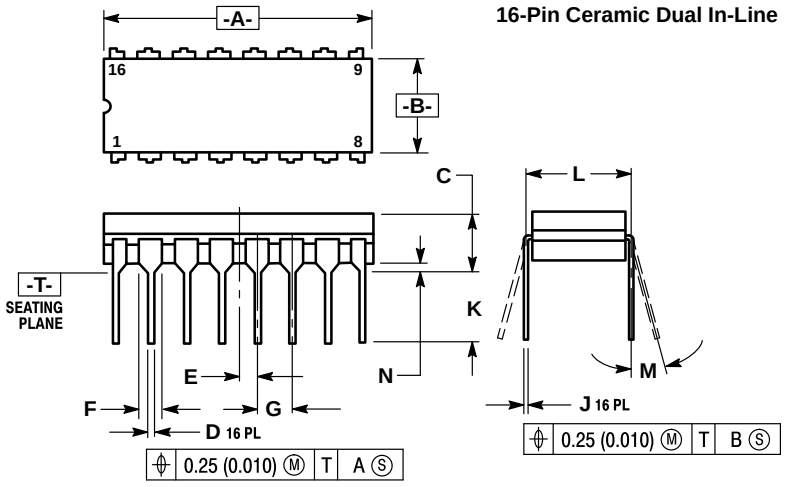
Case 648-08 N Suffix
16-Pin Plastic



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

Case 620-09 J Suffix
16-Pin Ceramic Dual In-Line



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

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* Η αρίθμηση είναι σύμφωνα με την αρίθμηση του adobe reader.